

(10) **Patent No.:** **US 6,563,331 B1**
(45) **Date of Patent:** **May 13, 2003**

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|--------------|-----------|------------------|---------|
| 5,313,156 A | 5/1994 | Klug et al. | |
| 5,650,732 A | * 7/1997 | Sakai | 324/754 |
| 5,865,319 A | 2/1999 | Okuda et al. | |
| 6,104,183 A | 8/2000 | Kobayashi et al. | |
| 6,313,652 B1 | * 11/2001 | Maeng | 324/760 |
| 6,314,332 B1 | * 11/2001 | Kida | 700/113 |

* cited by examiner

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(57) **ABSTRACT**

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An apparatus for testing semiconductor devices allows various testing processes, including a burn-in process, to be performed at the same testing stage. Test trays which contain the semiconductor devices are used throughout an in-line system so that an entire back-end process can be performed without loading/unloading the semiconductor devices between the various tests. The in-line system includes multiple test and burn-in apparatuses as well as a single sorting unit which performs a composite sorting operation after all the testing processes. A method for testing semiconductor devices in the in-line system includes testing the semiconductor devices in the test trays using the test and burn-in apparatus, transferring the test trays to a different testing apparatus for a second testing, and finally sorting the semiconductor devices after all testing processes have been performed based on a final sorting map created by combining test tray maps generated during each of the tests.

- (30) Foreign Application Priority Data

Dec. 26, 1997 (KR) 97-74610

(51) **Int. Cl.⁷** **G01R 31/02**

(52) U.S. Cl. 324/760; 324/765; 324/158.1;
209/574

(58) Field of Search 324/755, 754,
324/760, 765, 158.1; 209/573, 571, 574

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,184,068 A * 2/1993 Twigg et al. 324/755

26 Claims, 9 Drawing Sheets

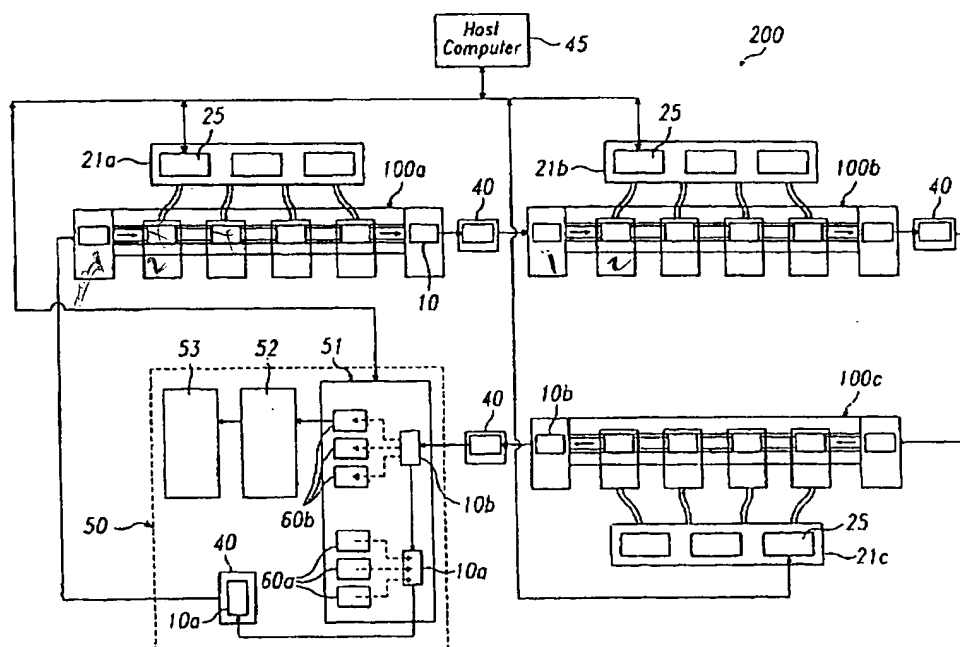


FIG. 1
(Prior Art)

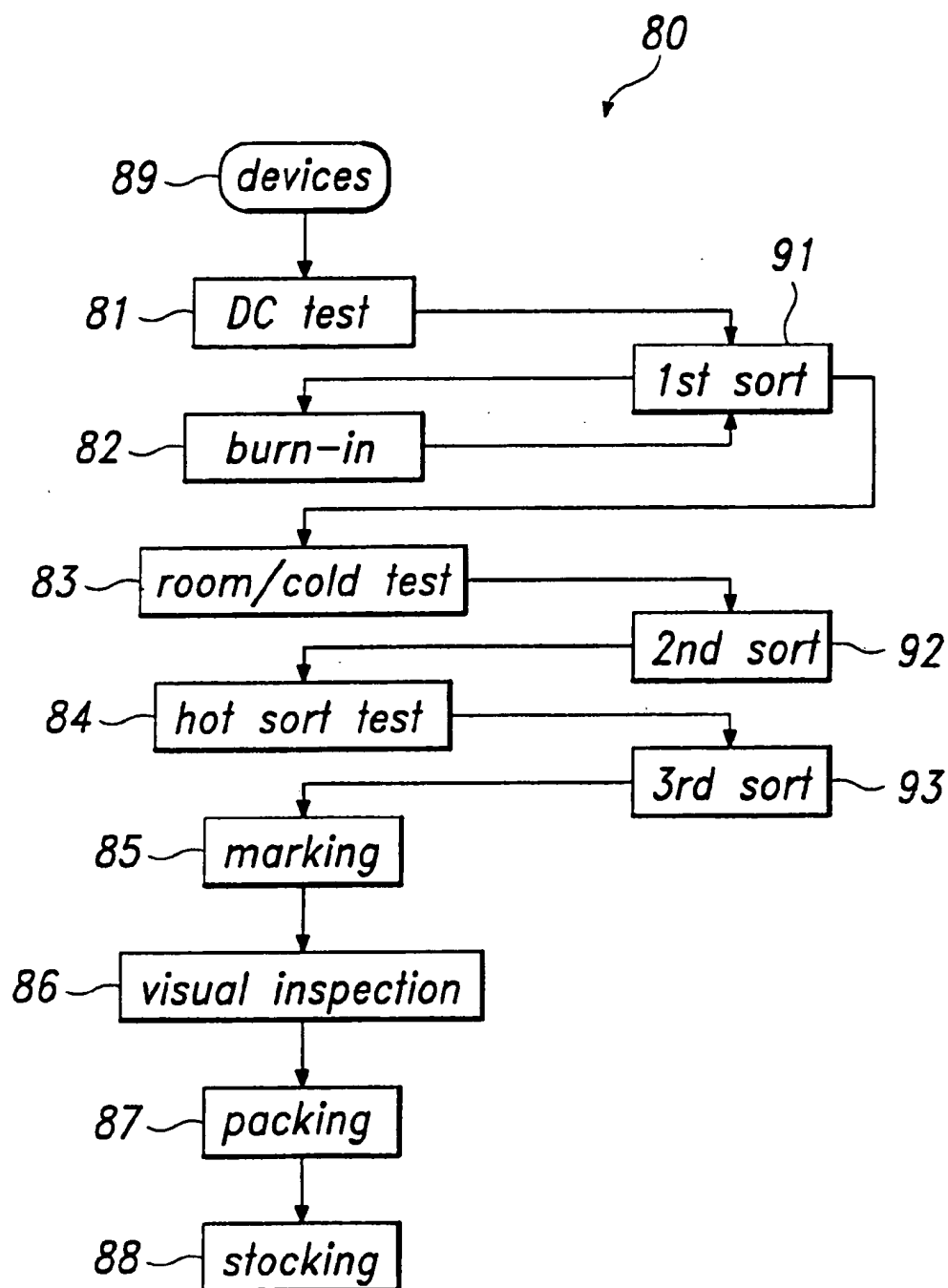


FIG. 2

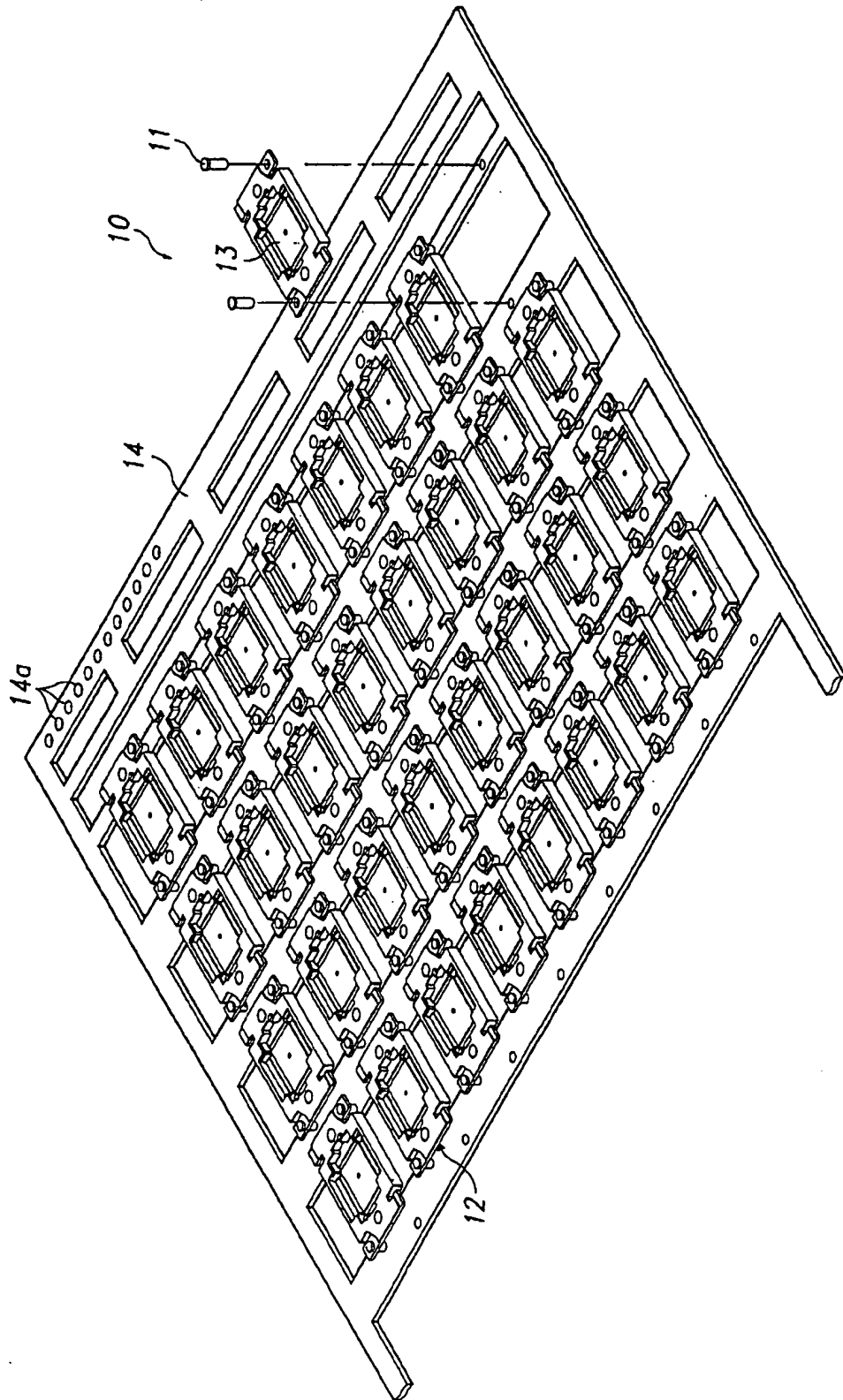


FIG. 3

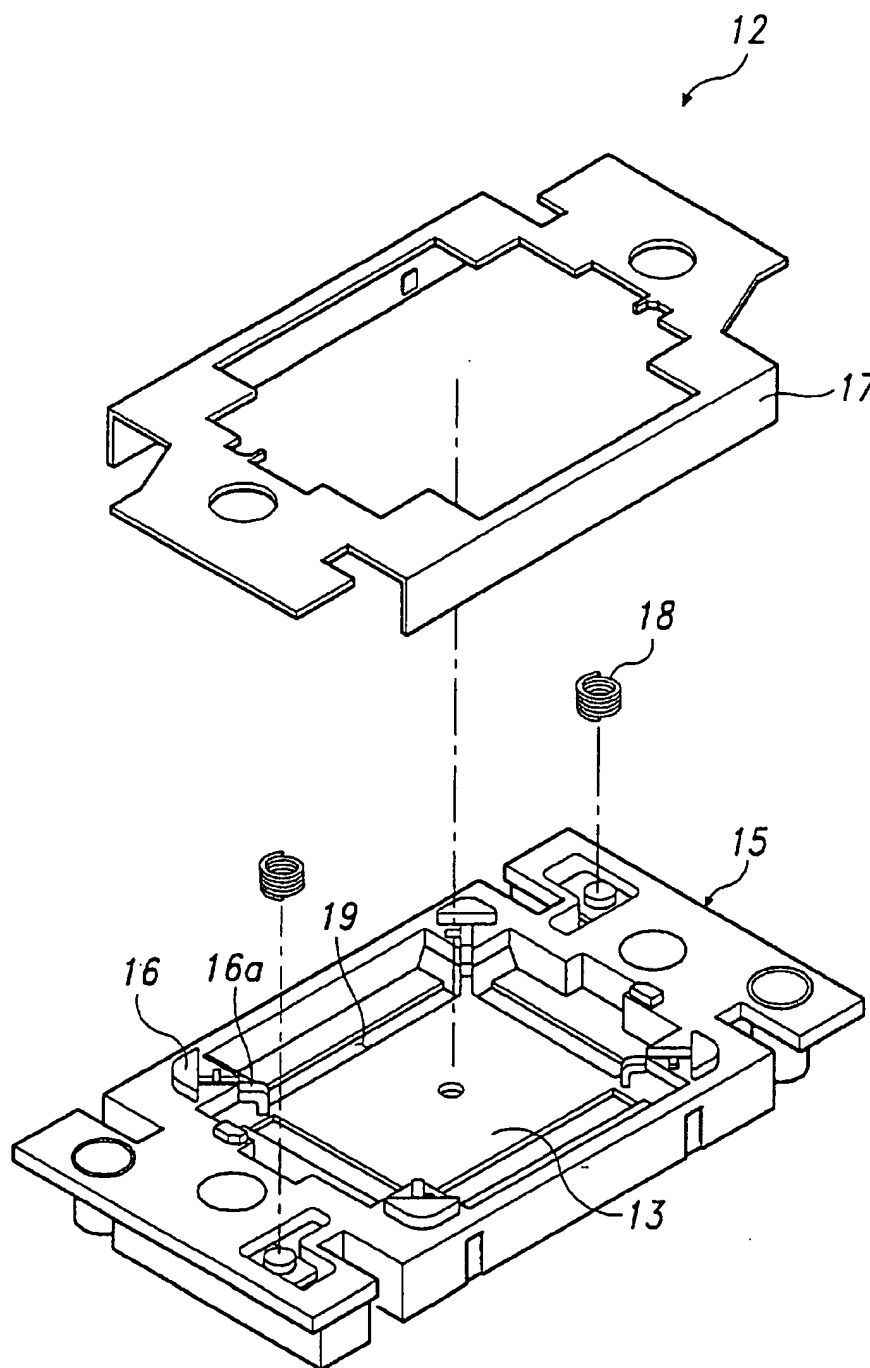


FIG. 4

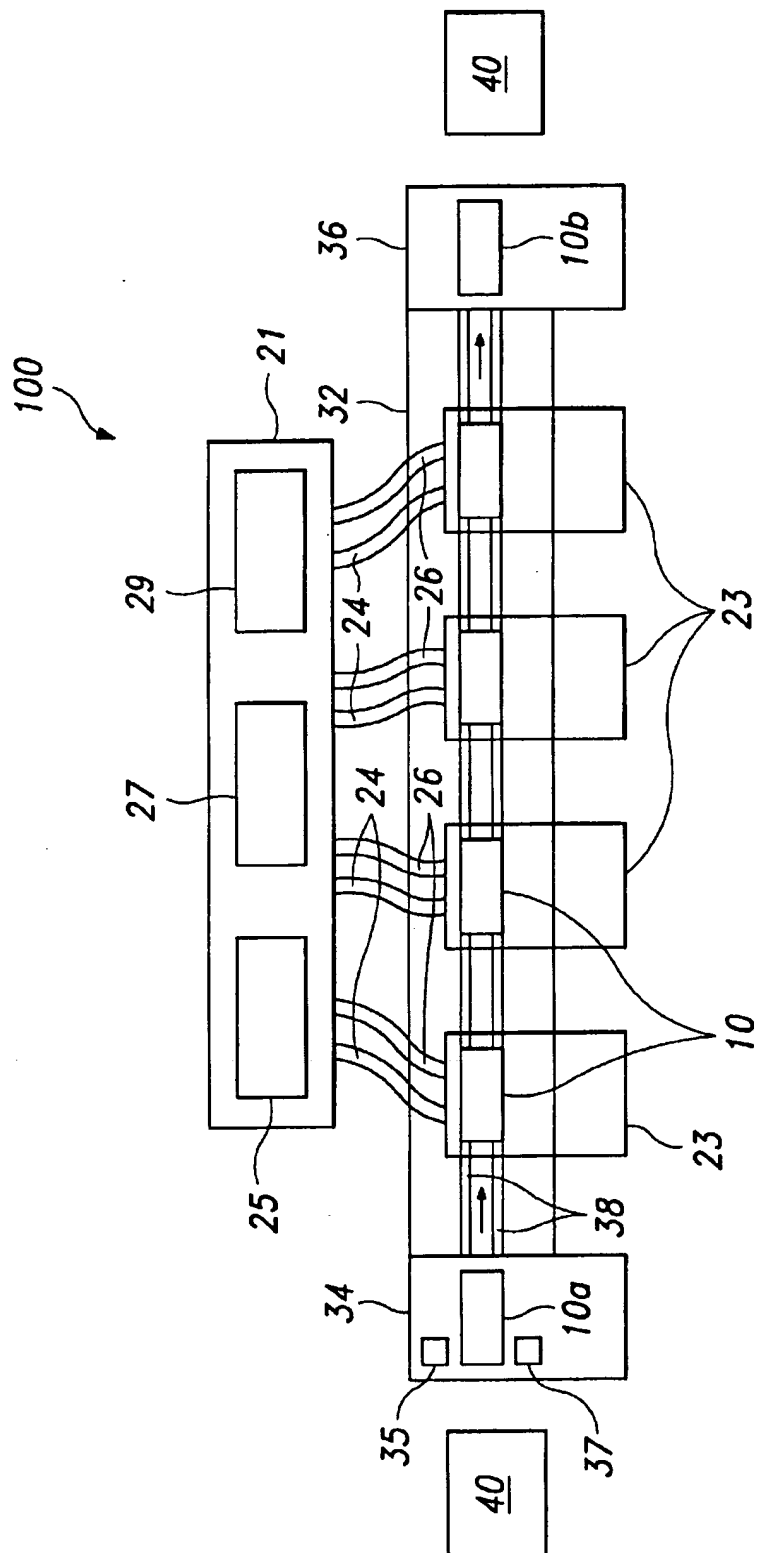


FIG. 5

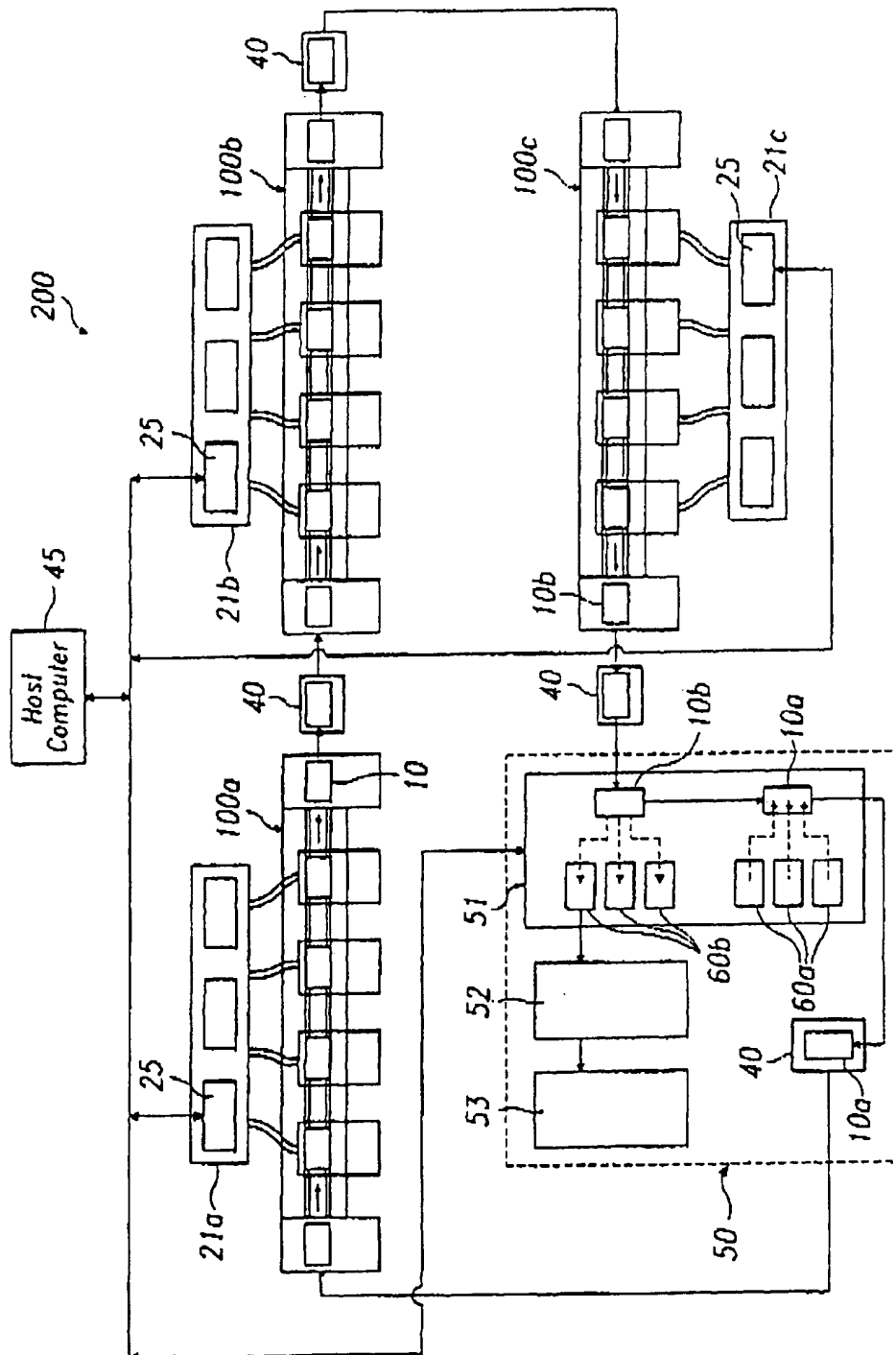


FIG. 6

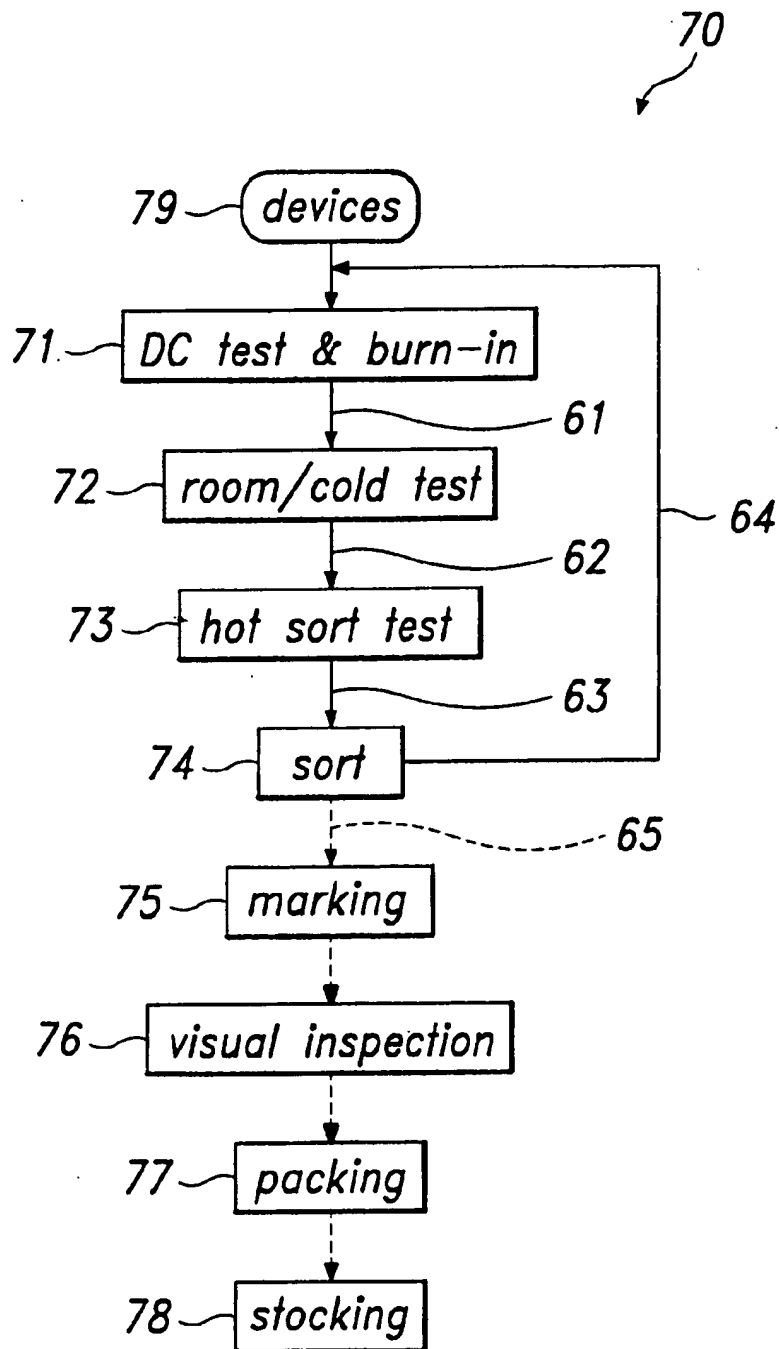


FIG. 7

120

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|----|--------|---|---|---|---|---|--------|
| 1 | 1 | ϕ | 1 | 1 | 5 | 5 | 1 | 1 |
| 2 | 1 | 1 | 1 | 8 | 1 | 1 | 1 | 1 |
| 3 | 21 | 1 | 1 | 1 | 4 | 5 | 6 | 6 |
| 4 | 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 6 | 1 | 1 | 1 | 1 | 5 | 7 | 8 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 8 | 1 | ϕ | 1 | 1 | 1 | 1 | 1 | ϕ |

4ea

124

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|----------------------|--------------------|--------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 1 | 1(1) | 2(R ₁) | 3(3) | 2(2) | 3(R ₁) | 2(BCD) | 1(1) | 1(1) |
| 2 | 1(1) | 1(1) | 1(1) | 8(R ₃) | 1(1) | 1(1) | 1(1) | 1(1) |
| 3 | 2(T _{III}) | 1(1) | 1(1) | 1(1) | 4(R ₃) | 5(R ₃) | 6(R ₃) | 6(R ₃) |
| 4 | 8(R ₃) | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) |
| 5 | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) | 8(R ₂) | 1(1) | 1(1) |
| 6 | 1(1) | 1(1) | 1(1) | 1(1) | 5(R ₃) | 1(R ₁) | 1(R ₁) | 1(1) |
| 7 | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) | 1(1) |
| 8 | 1(1) | 1(R ₁) | ϕ (R ₂) | 1(1) | 1(1) | 1(1) | 1(1) | ϕ (Bonus) |

4ea

FIG. 8

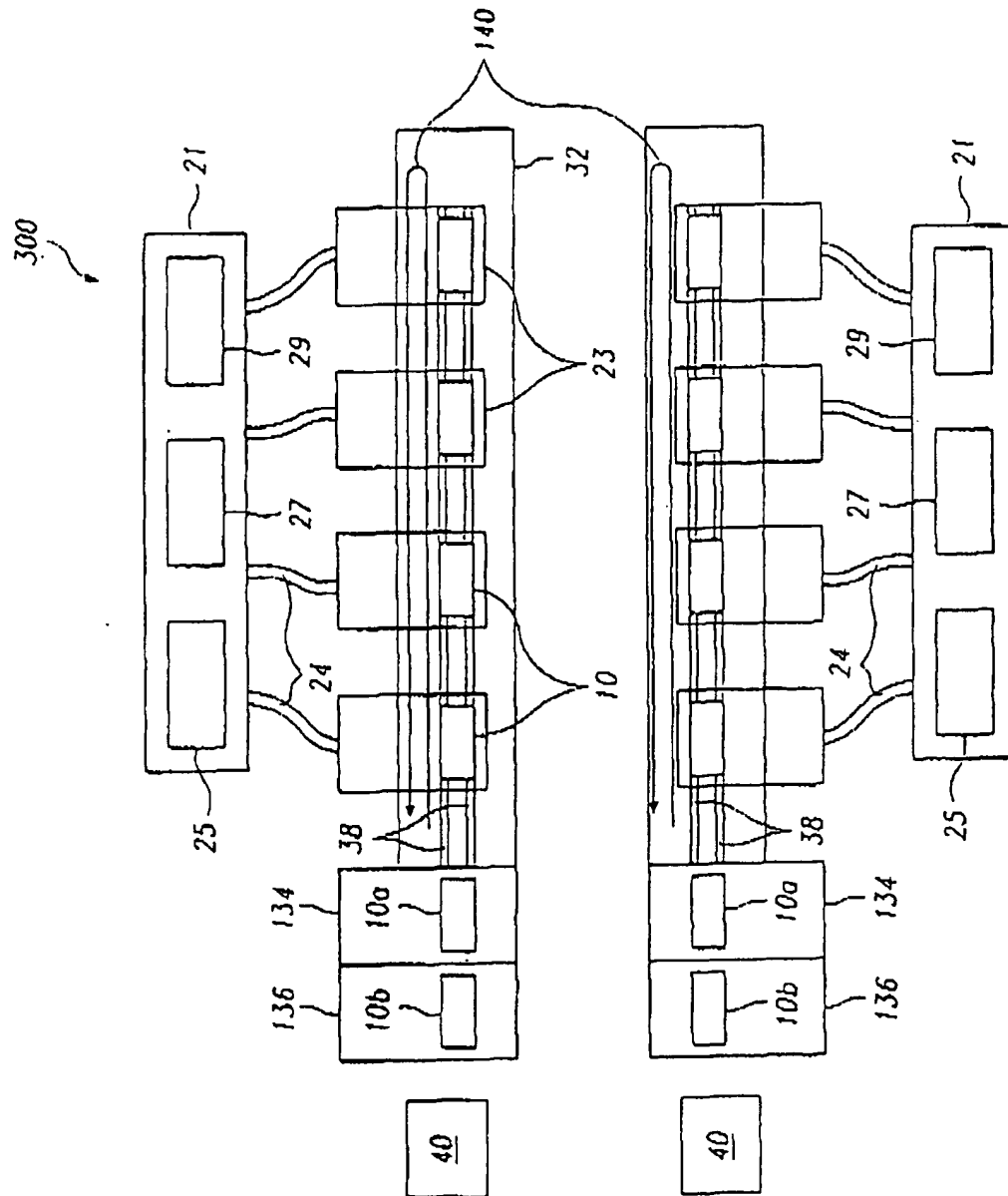
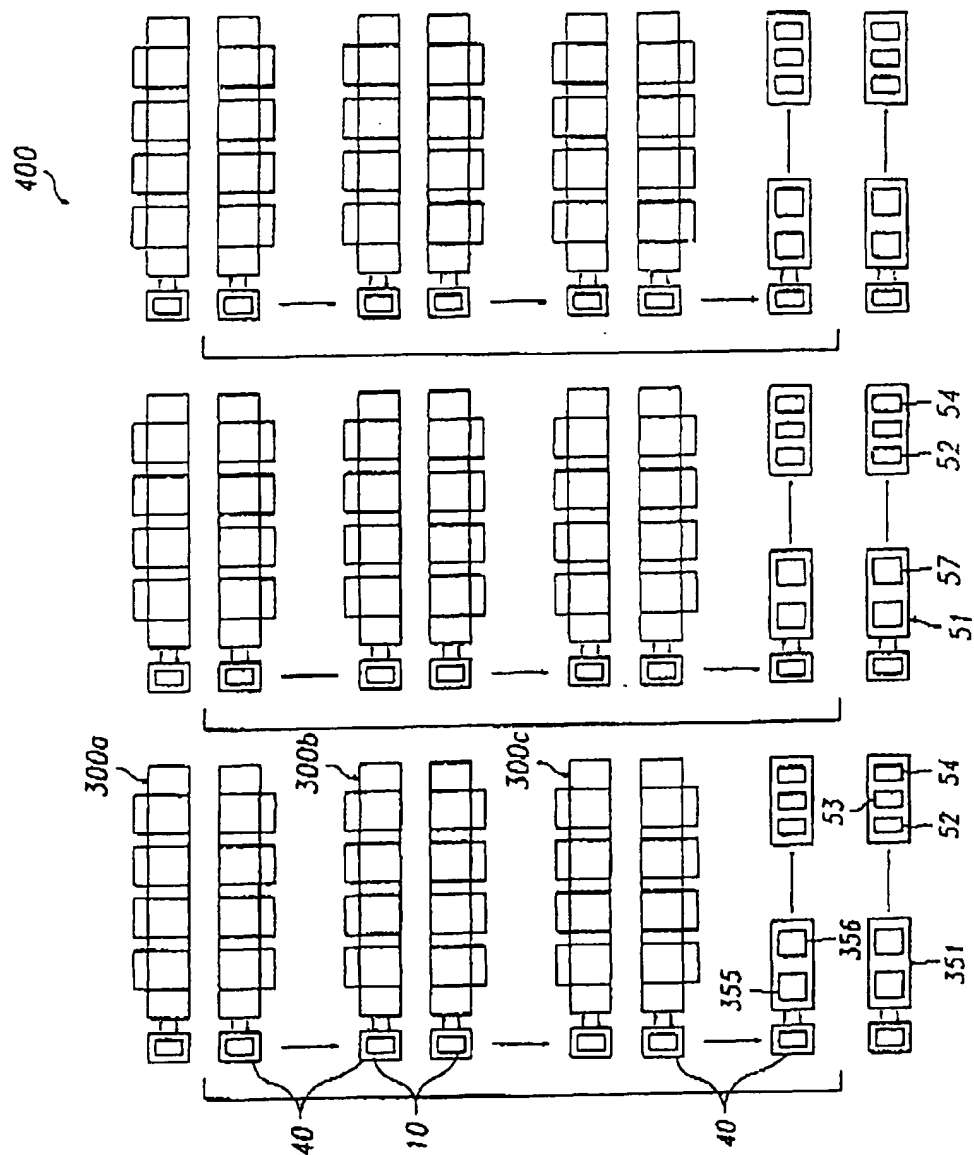


FIG. 9



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TEST AND BURN-IN APPARATUS, IN-LINE SYSTEM USING THE TEST AND BURN-IN APPARATUS, AND TEST METHOD USING THE IN-LINE SYSTEM

This application is a divisional of U.S. patent application Ser. No. 09/219,241 filed Dec. 22, 1998, now issued as U.S. Pat. No. 6,313,652; this application corresponds to Korean patent application No. 97-74610 filed Dec. 26, 1997 in the name of Samsung Electronics Co., Ltd., which is herein incorporated by reference for all purposes.

This application is related to Korean patent application No. 97-12256 filed on Apr. 2, 1997 entitled "Method for Generating Lot in Semiconductor Test Process System" which is herein incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to an apparatus and method for testing semiconductor devices. More particularly, the present invention relates to a test and burn-in apparatus for semiconductor chip package devices, an in-line system which includes the test and burn-in apparatus, and a test method which employs the in-line system.

2. Description of the Related Art

A manufacturing process for producing semiconductor devices generally includes three sub-processes: a wafer fabrication process; a package assembly process; and a back-end process. The wafer fabrication process encompasses the procedures for creating a large number of circuits on a thin disc, or wafer, of semiconductor material such as silicon. The package assembly process is the process by which an individual chip, having been separated from the wafer, is assembled into a package for establishing interconnections with a suitable operating environment. The back-end process includes several test steps where the packaged devices are tested to determine the parameters of the devices and whether the devices appropriately perform their intended function. The back-end process also includes sort steps in which the tested devices are sorted according to their individual parameters.

FIG. 1 is a flow chart illustrating a conventional back-end process 80 for manufacturing semiconductor devices 89. As shown in FIG. 1, the conventional back-end process 80 includes four test steps 81, 82, 83 and 84, three associated sort steps 91, 92 and 93, a marking step 85, a visual inspection step 86, a packing step 87, and a stocking step 88. The four test steps are performed in sequence and include a DC test 81, a burn-in step 82, a room/cold test 83, and a hot sort test 84.

The assembled semiconductor devices 89 are provided to the back-end process 80 in package form. Specifically, the assembled semiconductor devices 89 are loaded in a device tray and then provided to the DC test 81. The DC test 81 is performed to detect electrical failures which can occur during the package assembly process. After performance of the DC test 81, the first sort step 91 is engaged during which good devices in the device tray are transferred to a burn-in board, while failed devices are scrapped. The burn-in board, once supplied with the good devices, is transferred to the burn-in step 82.

The burn-in step 82 is an unusual test in which the semiconductor devices are subjected to extreme conditions (such as high temperature) in order to pre-screen out early device failures that might take place during actual usage.

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Following the burn-in step 82, the burn-in board is returned to the first sort step 91. The devices in the burn-in board are then sorted depending on the results of the burn-in step 82. The passing devices are again loaded in the device tray and transferred to the next test step. Although, for clarity, the first sort step 91 appears as single block in FIG. 1, several processes are actually carried out during this step. Specifically, these processes include: moving the semiconductor devices from the device tray to the burn-in board and from the burn-in board back to the device tray; scrapping the failed devices after the DC test 81; and sorting the devices after the burn-in step 82. In most cases, both the first sort step 91 and the DC test 81 are carried out at the same stage of the manufacturing process.

Following the burn-in step 82, the room/cold test 83 is performed. The room/cold test 83 begins after the good devices stored in the device tray are transferred to a room/cold tester. The room/cold tester includes a handler which shifts the devices from the device tray to a test tray. The room/cold test 83 is carried out at either about 25° C. (room temperature) or below 0° C. (freezing), so that DC failures or function failures can be checked. As the room/cold test 83 operation is completed, the devices in the test tray are again sorted, this time based on the room/cold test results. The good devices are shifted to the device tray which will carry the devices to the next test step while the failed devices are scrapped. The second sort step 92 is carried out by the handler of the room/cold tester. As described above, the test tray of the room/cold tester is used to carry the devices to and from the contact parts of the tester, while the device tray carries the devices between two testers.

The good devices in the device tray, having been room/cold tested, are then transferred to the hot sort test 84, which is performed under high temperature conditions, i.e., approaching about 83° C. The hot sort test 84, as is widely known in the art, verifies the electrical or functional characteristics of the devices and determines their operational speed. Similar to the room/cold test 83, the hot sort test 84 includes the additional steps of removing the devices from the device tray and placing them in the test tray, and then removing them from the test tray and placing them on the device tray. Moving the devices from tray to tray is carried out by a handler (that is, by handling equipment) of the tester. The third sort step 93 is associated with the hot sort test 84 and is performed together with the shifting of the devices by the handler after completion of the hot sort test 84.

When new semiconductor material arrives to be tested in the back-end process, it is handled by lot ID number. A human operator typically needs to input the lot ID number into the system in order to generate a test result and to measure the output obtained from a given input. Between the loading and unloading of the semiconductor devices, there are several general steps which take place inside the handler regardless of the test function being performed. These general steps require time to perform. Specifically, test tray index time, soaking hot or cold temperature processing time and sorting time must all be included in the overall device loading/unloading time during transfer between trays. The time requirements are even worse when rework is required following the main process. The total processing time includes a lot of preparation time during handler processing, even before actually testing the devices and combining the output. Additionally, a human operator has to count the total output and record the test results on every lot traveller card.

Unfortunately, as indicated above, conventional testers require additional equipment for transporting between test

steps and transferring between trays (handling) both the devices to be tested and those which have already been tested. Furthermore, shifting the devices between trays during every test step adds time and complexity but does not add any value in the performance of the tests. In other words, the complicated processes engaged in by the handler have no positive affects on the performance of the tests. In fact, the conventional handling requirements add cost and complexity to the semiconductor device manufacturing process without any corresponding benefits. Specifically, the prior art handlers increase significantly the space and time requirements for moving the devices through the back-end process, as well as the costs associated due to increased equipment requirements. Also, semiconductor devices being manipulated by the handler are faced with the possibility of considerable damage during movement between trays.

Another significant problem in the prior art is that the current burn-in testers require a long test time. The excessive test time is further compounded by the amount of time it takes to transfer the devices between the burn-in board and the device tray, the time it takes to load and unload the burn-in board, and the time it takes to raise or drop the test temperature and/or to check the burn-in process or signals. In addition, the burn-in board and its test sockets are high-priced expendables. Accordingly, all of the above-discussed testing steps—which are required for every semiconductor device—impose a heavy cost burden on the end-consumer.

Finally, typical burn-in testers perform at a slow test rate and a low test accuracy. The reason why the test rate of typical burn-in testers is slow is that test signals are applied in parallel to the devices in every row or every column through circuit patterns on the burn-in board. This testing technique makes it difficult to apply test signals to the specific device to be tested.

Furthermore, typical burn-in testers have a long serial scanning time when compared with normal testers. For example, JEC Co.'s burn-in tester model no. MBT P1700S has a test rate of 4 MHz maximum and a transition time of approximately 50 ns, which represents a long cycle time. This tester is therefore capable of performing a few of the desired tests, such as a gross function test or a long cycle test, in addition to the burn-in step 82. It is unable, however, to perform either the room/cold test 83 or the hot sort test 84, both of which require shorter cycle testing times.

Another major problem in the prior art involves the prior art retest procedures. The prior art retest is a serial-type retest which means it is performed on the same machine as the initial test for each of the different test steps. Using this type of retest adds to the time requirements and complexity of the back-end process.

As a consequence of all of these drawbacks, it is considerably difficult to systemize the back-end process of the in-line system. Use of the prior art processes and equipment results in dropped productivity and lost cost-efficiency. Accordingly, improvements in the back-end process are extremely desirable in light of the industry desire for higher device throughput and lower manufacturing costs. In addition, it would be particularly desirable to eliminate the need for three separate sort steps, in order to further increase throughput and lower costs.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an improved testing apparatus for semiconductor devices, which allows various tests of a back-end process, including a burn-in process, to be performed at the same platform.

It is another object of the present invention to provide a back-end process which uses an in-line system throughout the entire process and which employs more space-efficient equipment.

It is still another object of the present invention to provide an improved testing method which includes a burn-in process having a reduced number of steps, requires less time to perform, and uses equipment occupying less space.

It is yet another object of the present invention to provide a testing system which eliminates the unnecessary movement of semiconductor devices between trays by employing test trays which are directly transferable between test steps.

It is still another object of the present invention to provide a single composite sort step which eliminates the need for multiple sort steps between each of the various tests and burn in processes.

It is yet another aspect of the present invention to provide a parallel-type retest, rather than a serial-type retest, which is independent of the testing machine and which uses previous test results and data automation to efficiently retest the devices.

These and other objects of the present invention are attained by using a test and burn-in apparatus for semiconductor devices. In particular, the test and burn-in apparatus in accordance with the present invention includes a rail for transferring multiple test trays, each of which contains multiple semiconductor devices to be tested. The apparatus also includes a loader for loading the test trays onto the rail and a unloader for unloading the test trays from the rail. Furthermore, the apparatus comprises a chamber, which the rail traverses. The test trays are provided in the chamber along the rail, so that the semiconductor devices contained in the test trays may be subjected to a test and/or burn-in process within the chamber. A plurality of test heads are formed in the chamber so that each test head can be electrically connected to a respective one of the test trays to perform the test and/or burn-in process for the semiconductor devices.

The apparatus may further include a main frame which includes a control unit which is electrically connected to the test heads. The main frame may further include a coolant refrigerator unit for cooling down the test heads. The number of test heads included is preferably either four or eight, with each test head capable of performing the test and/or burn-in process for sixty-four semiconductor devices in a single test tray. Preferably, the devices to be tested are semiconductor chip packages with gull-wing leads, or chip scaled packages.

According to an alternate aspect of the present invention, an in-line system is provided for manufacturing semiconductor devices. The in-line system includes a plurality of test and burn-in apparatuses, a transferring member, and a sorting unit. Each test and burn-in apparatus performs a different test and/or burn-in process from the other and includes a rail for transferring multiple test trays between processes. Each test tray holds a plurality of semiconductor devices. Each test and burn-in apparatus further includes a loader for loading the test trays onto the rail and a unloader for removing the test trays from the rail. Additionally, the rail traverses through a chamber in which the test or burn-in process takes place. Accordingly, the test trays travel in the chamber along the rail, and the plurality of semiconductor devices contained in the test trays are then subjected to the test or burn-in process.

A plurality of test heads are formed in the chamber where the test and/or burn-in process for the semiconductor devices

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is performed. Each of the test heads corresponds to a respective one of the test trays in the chamber, and each test head is electrically connected to its corresponding test tray. The transferring member receives the test trays from the unloader of one test and burn-in apparatus and supplies them to the loader of another test and burn-in apparatus. Accordingly, the test and burn-in apparatuses are linked in an in-line system by the transferring member. The semiconductor devices which pass all of the tests and burn-in processes of the in-line system are transferred to device trays from the test trays by a sorting unit.

Each test and burn-in apparatus in the in-line system further includes a main frame which includes a control unit electrically connected to the test heads. The control units and the sorting unit can be electrically connected to each other. The main frames can further include a coolant refrigerator unit for cooling down the test heads. The in-line system preferably includes four or eight test heads in each test and burn-in apparatus, with each head being capable of performing the test and/or burn-in process for sixty-four semiconductor devices in one test tray. The semiconductor devices are preferably semiconductor chip packages with gull-wing leads.

In particular, the in-line system according to this invention preferably includes a first test and burn-in apparatus for performing a DC test and a burn-in process, a second test and burn-in apparatus for performing a room/cold test, and a third test and burn-in apparatus for performing a hot sort test. Moreover, a sorting unit is preferably provided which can perform two operations: first, moving the devices which have already been tested from a test tray to a device tray; and second, providing new devices, which have not yet been tested, from a new device tray to the test tray.

According to still another aspect of the present invention, a method is provided for testing semiconductor devices. This method includes providing a test tray containing multiple semiconductor devices to a first test and burn-in apparatus. Next, a first testing process is performed on the semiconductor devices contained in the test tray in the first test and burn-in apparatus. The test tray is then transferred from the first test and burn-in apparatus to a second test and burn-in apparatus. A second testing process is then performed on the semiconductor devices contained in the test tray in the second test and burn-in apparatus. The test tray is next transferred from the second test and burn-in apparatus to a third test and burn-in apparatus. Subsequently, a third testing process is performed on the semiconductor devices contained in the test tray in the third test and burn-in apparatus. The test tray is then transferred from the third test and burn-in apparatus to a sorting unit where the semiconductor devices in the test tray are sorted based on the results of the three tests and delivered to a device tray during a sorting process.

The test and burn-in apparatuses and the in-line system described previously are preferably employed in carrying out this method, with each apparatus performing one of the three testing steps. Each of the transferring steps may be conducted by a transferring member which receives the test tray from the unloader of one apparatus and supplies it to the loader of the next apparatus, such that all of the apparatuses are linked together via the in-line system's transferring device.

In the previously described method, each test and burn-in apparatus can further include a main frame which includes a control unit electrically connected to test heads within the apparatus. Furthermore, the control units may be electrically

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connected to each other and to a sorting unit where the sorting process for sorting the semiconductor devices in the test tray is conducted. In particular, semiconductor device selection during the sorting process is preferably based on test tray maps which have been recorded as a result of the three testing steps and transmitted to the sorting step via the control units.

In addition, the method can further include loading new semiconductor devices contained in a new device tray into the test tray from which the tested semiconductor devices have just been sorted, and providing that test tray containing the new devices to be tested to the first test and burn-in apparatus for testing. Also, the first, second and third testing processes may include a burn-in process, a room/cold test and a hot sort test, in various orders. The third testing process is preferably the hot sort test, however.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flow chart illustrating a conventional back-end process for manufacturing semiconductor devices.

FIG. 2 is a perspective view of a test tray which can be used in accordance with a test and burn-in apparatus according to the present invention;

FIG. 3 is an exploded view of an insert of the test tray shown in FIG. 2;

FIG. 4 is a schematic view of a first preferred embodiment of a test and burn-in apparatus in accordance with the present invention;

FIG. 5 is a schematic view of an in-line system employing the test and burn-in apparatus shown in FIG. 4, in accordance with the present invention;

FIG. 6 is a flow chart illustrating a back-end process using the in-line system of FIG. 5, according to a preferred embodiment of the present invention;

FIG. 7 is a view illustrating test tray maps employed in the back-end process of the present invention;

FIG. 8 is a schematic view of a second preferred embodiment of a test and burn-in apparatus in accordance with the present invention; and

FIG. 9 is a schematic view of an in-line system employing the apparatus shown in FIG. 8, in accordance with the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

The preferred embodiments of the present invention will now be described more fully with reference to the accompanying drawings, in which like numerals represent like elements. It should be noted, however, that this invention may be embodied in many different forms and the claims should not be construed as being limited to the embodiments set forth in this description. Rather, these embodiments are provided by way of illustration only, so that the disclosure will be thorough and complete and convey the spirit but not scope of the invention to those skilled in the art. The scope is limited solely by the claims.

Various tests are required for ensuring the proper functioning of semiconductor devices. These tests are performed using one or more test and burn-in apparatuses in accordance with the present invention. In particular, the test and burn-in apparatuses (TABI) are so called because in the present invention, they enable a burn-in process in addition to the typical semiconductor device tests (i.e., a DC test, a room/cold test, and a hot sort test) to be performed in the

same apparatus. Therefore, the testing apparatus of the invention will be referred as a test and burn-in (TABI) apparatus below.

FIG. 2 is a perspective view of a test tray 10 while FIG. 3 is an exploded view of an insert 12 of the test tray 10 shown in FIG. 2. Referring to FIGS. 2 and 3, the test tray 10 is employed to carry semiconductor chip packages throughout the back-end process. The test tray 10 can be designed to hold any type of chip device, however, the semiconductor chip packages preferably consist of gull-wing leads, such as quad flat packages (QFPs) or thin small outline packages (TSOPs). Additionally, chip scaled packages (CSPs) such as μ -BGA, which have been recently developed and proposed in the art, can be employed in the test tray 10.

The test tray 10 includes a plurality of inserts 12, provided within a tray frame 14, to contain the semiconductor devices. According to this embodiment, the test tray 10 has sixty-four inserts 12. However, test trays having a different number of inserts (i.e., one hundred twenty-eight, two hundred fifty-six, or five hundred twelve) can be used alternatively. Each insert 12, which is fixed (either removably or permanently) to the tray frame 14 by fasteners 11, accommodates one semiconductor device. Additionally, tray ID holes 14a are used to generate a tray ID number, a more detailed description of which will follow later.

The insert 12 is made of a body 15 and a pushing element 17. The pushing element 17 is elastically joined above the body 15 by springs 18. A pad 13, positioned in the center of the body 15, is formed for receiving and supporting the semiconductor chip package (i.e., a QFP or TSOP). The pad 13 is connected to the body 15 at its corners, with four slits 19 at its edges. Four latches 16 are also provided, corresponding to each of the corners of the pad 13. Each of the latches 16 has a hook 16a which is pivoted at a lower end of the latch 16.

By pushing down on the top of the pushing element 17, the latch 16, which is in contact with the bottom surface of the pushing element 17, is also moved downward, and the hook 16a is caused to rotate upwardly. The insert 12 can then receive the semiconductor device onto the pad 13. After the device is positioned, when the pushing force is removed, the pushing element 17 and the latch 16 are returned to their original position by the action of the springs 18. The hooks 16a are also returned to their original positions by rotating downwardly such that the device now located on the pad 13 is secured by the hooks 16a. Furthermore, leads of the device are exposed through the slits 19, so that the device can be tested through a contact between the device leads and a tester.

FIG. 4 is a schematic view of one embodiment of the test and burn-in (TABI) apparatus 100 in accordance with the present invention. As shown in FIG. 4, the TABI apparatus 100 includes a rail 38 for transferring test trays 10. Each test tray 10 contains a plurality of semiconductor devices which are to be tested. The TABI apparatus 100 further includes a loader 34 and an unloader 36 which are located, respectively, at both ends of the rail 38. New trays 10a, holding devices which have not yet been tested, are loaded onto the rail 38 by the loader 34. The unloader 36 is provided to unload tested trays 10b, containing already tested devices, from the rail 38. The new trays 10a, test trays 10 and tested trays 10b are the same test trays, but at different steps in the testing process.

A chamber 32, which at least partially encloses the rail 38, includes four test heads 23 which are formed in the chamber 32. The test trays 10 travel into the chamber 32 along the rail

38, and are then stopped for testing. Testing is performed by electrically connecting each of the semiconductor devices in one of the test trays 10 to one of the test heads 23. The chamber 32 applies heat or cooling to the test heads for a proper test and/or burn-in temperature. Accordingly, all of the devices in every test tray are subjected to a test and/or burn-in process within the chamber 32, by being electrically connected to the test heads 23.

The test heads 23 are also connected to a main frame 21 which includes a control unit 25, a coolant refrigerator unit 27, and a power source 29. The control unit 25 controls the functioning and sequence of the testing operations of the test heads 23. The power source 29 supplies electrical power to the test heads 23. Both the control unit 25 and the power source 29 are electrically connected to the test heads 23 by cables 24. The coolant refrigerator unit 27 is connected to the test heads 23 by hoses 26 and is thereby able to supply chilled water in order to cool down the test heads 23 (particularly on a high-speed board). A transferring member 40, such as a cart, receives the test trays 10 from the unloader 36 and then supplies them to the loader 34.

The TABI apparatus 100 according to this embodiment therefore permits the testing of two hundred and fifty-six semiconductor devices at a time, since the TABI apparatus 100 has four test heads 23, each of which is connected to one test tray 10 holding sixty-four semiconductor devices. However, by modifying the number of the test heads 23 and/or the number of devices per tray, the apparatus 100 can be configured to test more or less devices at a time, as desired. Additionally, while the TABI apparatus 100 of this embodiment has only one main frame 21 and one chamber 32, several other configurations are also possible. For example, two main frames and two chambers or one main frame and two chambers are other possible configurations.

Operation of the TABI apparatus 100 of this embodiment is as follows. First, the new trays 10a, holding the devices to be tested, are loaded onto the rail 38 from the transferring member 40 by the loader 34. Next, each new tray 10a moves along the rail 38 and into the chamber 32 and is located on one of the test heads 23. The test and/or burn-in process is then performed within the chamber 32 when the devices in the test trays 10 and the contact parts in the test head 23 are electrically connected to each other. The tested trays 10b, containing the tested devices, are then moved toward the unloader 36 along the rail 38. The tested trays 10b are unloaded from the rail by the unloader 36 and then transferred to the next process by the transferring member 40.

As described above, the ability to use the test trays themselves to transport the semiconductor devices through the entire testing process, without requiring transfer of the devices to and from device trays between tests, is one of the novel and improved features of the testing apparatus of the invention. The absence of several device trays for the same devices results in reduced cost and space requirements for the apparatus (i.e., reduced by the amount of money and space required for the handler of the prior art). It also results in significantly less handling time being taken to handle the trays. An additional novel feature of the present invention is that the TABI apparatus of this invention allows a burn-in process as well as other kinds of electrical tests to be performed within a single apparatus by independently transmitting test signals to the devices. Both of these novel features help to reduce the number of steps required in the back-end process and help make it possible to realize an in-line system for carrying out the entire back-end process.

When the TABI apparatus 100 is to be used for testing under high temperatures, such as in the burn-in process or

the hot sort test, the TABI apparatus 100 of the present invention may further include a pre-heater 35. The pre-heater 35 applies heat to the semiconductor devices that are being loaded onto the rail 38 by the loader 34. On the other hand, the apparatus 100 may also include a pre-cooler 37 for the low temperature testing processes. The pre-heater 35 and pre-cooler 37 can alternatively be located in each test head 23.

Many different types of testers are available for use with the present invention. In particular, the TABI apparatus 100 in accordance with the present invention can employ a well-known tester made by the Schlumberger Co. The Schlumberger tester is basically equipped to accommodate four test heads, and is also able to allow sixty-four parallel fan-outs in each pin slice board (i.e., a timing board). It is therefore possible to perform the test and/or burn-in process on two hundred and fifty-six semiconductor devices at the same time. Additionally, an algorithmic pattern generator integrated circuit (APG IC) has been developed for attaining a test rate of about the 200 MHz level, and a high speed timing module with overall timing accuracy has also been developed. Moreover, the capacity of the simultaneous parallel test has increased to two hundred fifty-six parallel from sixty-four parallel. Accordingly, one may likewise expect an increase in the number of the devices which are capable of being tested at once in each test and burn-in apparatus of this invention.

FIG. 5 depicts the in-line system 200 in a back-end process. A plurality of TABI apparatuses according to the invention may form the in-line system 200, as illustrated in FIG. 5. Referring to FIG. 5, the in-line system 200 includes three TABI apparatuses 100a, 100b and 100c, and only one sorting unit 51. Each TABI apparatus 100a, 100b or 100c is substantially the same as the apparatus depicted in FIG. 4, however, each apparatus 100a, 100b or 100c in the in-line system 200 performs a different testing process than the other apparatuses. The sorting unit 51 provides the ability to sort the devices from each tested tray 10b and to transfer the sorted devices to a separate device tray 60b, according to test results of each testing process. The in-line system 200 may also include other units in the back-end process, such as a marking unit 52 and a visual inspection unit 53, due to the similar unit per hour (UPH) capability between them and the sorting unit 51. The sorting unit 51, the marking unit 52, and the visual inspection unit 53 are preferably provided in one machine 50.

The in-line system 200 further includes a transferring member 40 such as a cart, a transfer rail, a conveyor belt, or an automated guide vehicle (AGV), for example, as is well known in the art. The transferring member 40 receives one or more test trays 10 from one apparatus and supplies them to another apparatus, whereby multiple apparatuses are linked together as an in-line system by the activity of the transferring member 40. The device trays as used in the prior art are therefore not required since the test trays 10 are transferred directly by the transferring member 40 to each of the subsequent testing apparatuses. The in-line system according to this invention can have the preferred configuration shown in FIG. 5, however, other configurations can also easily be adapted. The apparatuses could be configured to stand in a row, for instance.

The three TABI apparatuses 100a, 100b and 100c of the in-line system 200 each perform different test steps. For example, a DC test and burn-in process may be performed by one apparatus, a room/cold test may be performed by another apparatus, and a hot sort test may be performed by yet another apparatus. Although any of the apparatuses

could be configured to perform any of these test steps, it is preferable to configure the in-line system to perform the tests in the following order: first, the DC test and burn-in process; second, the room/cold test; and third, the hot sort test. Other sequences are also possible, however. For example, the room/cold test could be performed first, the DC test and burn-in process could be performed second, and the hot sort test could be performed third. Even performance of the burn-in process last is possible, provided the same test items as the room/cold test or the hot sort test are tested in the burn-in process.

The test results and other information obtained from each test step are sent to a host computer 45 through a network, and then transmitted to the sorting unit 51 in the form of test tray maps 120, as illustrated in FIG. 7. Referring to FIG. 7, the test tray maps 120 are log sheets in the form of computer files where the test results and other information from each of the tests is recorded. The test tray maps 120 may also be referred to as link-chained test tray maps. A more detailed description regarding the test tray maps 120 will follow later.

Again referring to FIG. 5, after the devices have been subjected to all of the test and burn-in processes, the sorting unit 51 proceeds to perform an off-line sorting so that all of the devices can be sorted from the tested trays 10b into an appropriate one of the device trays 60b. The sorting process is done according to the test results and other information recorded in the test tray maps 120 (see FIG. 7). The sorting unit 51 therefore performs two operations. One operation is moving the tested devices from the tested trays 10b to the device trays 60b according to the results of the test and burn-in processes; in other words, the above-described sorting process. The other operation performed by the sorting unit 51 is providing new devices, which have not yet been tested, from new device trays 60a to the new trays 10a. Dotted arrows in the sorting unit 51 represent the movement of the devices.

Following the sorting process, the device trays 60b are then supplied to the marking unit 52 by a conveyor belt, transfer rail, or other transferring member 40b, while the new trays 10a are supplied to the first TABI apparatus 100a by the transferring member 40. Contrary to the prior art in which loading and unloading of the devices is done at every tester, in the present invention, loading and unloading of the devices to transfer them between two trays is done only at the sorting unit 51.

Although the sorting unit 51 is illustrated as a single unit in FIG. 5, two or more sorting units can be selectively adapted for adjusting throughput to the TABI apparatus. Furthermore, the loading of new devices can alternatively be done in a place separate from the sorting unit 51. The separation of the sorting and loading functions is particularly preferable when dealing with large-sized lots having a large number of devices.

One of several advantages of the in-line system 200 according to this invention is the time savings resulting from the ability to quickly raise or drop testing temperature. The in-line system 200 also saves time in sorting the devices since the multiple sort steps of the prior art are reduced to a single step. Additionally, the reduction of the number of processes and the automation of the overall test process significantly reduces the possibility of damage during management of the devices and further protects against the problem of device damage caused by electrostatic discharge (ESD) resulting from workers or equipment coming into contact with the devices.

FIG. 6 is a flow chart which illustrates an overall back-end process 70 which uses the in-line system 200 of the present

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invention as shown in FIG. 5. With further reference to FIG. 5, and with additional reference to FIG. 6, the back-end process will be discussed. Assembled devices which are ready to be tested are provided to the in-line system 200 of the back-end process during a loading step 79. During the loading step 79, the devices are loaded into the new trays 10a from the device trays 60a. The new trays 10a are then transported by a transferring member 40a to the first TABI apparatus 100a which performs a DC test and burn-in process 71 on the devices. The devices contained in the test trays 10 are next transported by the transferring member 40 to a second apparatus 100b where a room/cold test 72 is performed and then to a third apparatus 100c where a hot sort test 73 is performed.

Accordingly, when each test and/or burn-in process 71, 72 and 73 is done, the test trays 10 are transferred to next test step 72 or 73, or to a sort step 74 by the transferring member 40. In other words, the transferring member 40 receives the test trays 10 from an unloader of the apparatus 100a, 100b or 100c and then supplies the test trays 10 to a loader of the next apparatus. The arrows designated by reference numerals 61, 62 and 63 in FIG. 6 represent the transfer pathway of the test trays 10 between steps.

Meanwhile, control units 25 (see FIG. 4) of each apparatus 100a, 100b and 100c are electrically connected both to each other and to the sorting unit 51 through a network including the host computer 45. The test results and other information obtained during the test steps 71, 72, and 73 can therefore be transmitted to the sorting unit 51 from the apparatuses 100a, 100b and 100c via the host computer 45. As previously described, the test results and other information produced at the test steps 71, 72 or 73 are recorded on the test tray maps 120 (see FIG. 7). A sort step 74 of the devices is carried out according to these test tray maps 120, such that all good devices in the tested trays 10b will be shifted to the device trays 60b.

After the sort step 74, empty test trays on the sorting unit 51 become new trays 10a and are transferred back to the loading step 79 to receive new devices (i.e., a new lot) from new device trays 60a having a new lot number. The entire back-end process thereby begins for the new lot. The process of returning the new trays 10a from the sorting step 74 to the loading step 79 is indicated by the solid line 64. Each of the solid arrows in FIG. 6 indicates movement of the test trays 10, 10a or 10b.

Meanwhile, the device trays 60b, which receive the good devices from the sorting unit 51, are supplied to the marking unit 52 so that a marking step 75 can be performed. This transfer is indicated by dotted line 65. The dotted arrows in FIG. 6 indicate movement of the device trays 60a or 60b.

As mentioned earlier, one of the greatest benefits of this invention is that it allows the back-end process for testing and sorting semiconductor devices to proceed in an in-line system. One of the main reasons why the invented process is able to proceed successively, namely, as an in-line process, is that only one set of trays, i.e., the test trays, are required during the testing procedures. No transfer between trays is required between testing steps. Another substantial benefit of this invention, which will be more fully described below, is that data automation using the link-chained test tray maps feature allows for the performance of a single composite sort step, as opposed to the multiple sorting steps required by the prior art.

Referring to FIG. 7, the link-chained test tray maps 120 will now be discussed in further detail. FIG. 7 illustrates a group of test tray maps 120 and subgroups of maps (or map

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sheaves) 122 and 124 employed in the test process of the present invention. Test results and other information (or mapping signals) obtained from each of the test and/or burn-in processes are transmitted to the host computer 45 (see FIG. 5) via the control units 25 (see FIG. 4) of the TABI apparatuses. These mapping signals are processed by the host computer and recorded in the test tray maps 120. The test tray maps 120 therefore contain the testing information concerning each of the devices in the test trays, specifically, whether they passed or failed each of the tests. These maps are therefore essential when sorting the devices.

Generation and assignment of the test tray maps 120 begins with determining a lot ID number and a tray ID number. When the devices are loaded into the new tray 10a (see FIG. 4), the test tray receives the lot ID number from the operator. The test tray also has a tray ID number defined by tray ID holes 14a (see FIG. 2) or a bar code. The host computer 45 (see FIG. 5) determines the tray ID number by sensing the tray ID holes 14a or the bar code of the test tray. The tray ID holes 14a, each of which is either punched or filled, represent a binary number which is translated into a decimal tray ID number by the host computer 45 (see FIG. 5). For example, twelve tray ID holes can represent a decimal tray ID number of between 0000 to 4095.

Once the tray ID number is recognized, the computer generates the tray map 120 along with a corresponding a map file name. The map file name is a combination of the tray ID number and the lot ID number. Therefore, although the same test tray is used for each lot, and hence the same tray ID number, the map files for that tray are distinguished from one another using the lot ID number. Examples of the map file name in relation to the tray ID holes are demonstrated in Table 1.

TABLE 1

Examples of the map file name.

| Tray ID Holes | Tray ID Number | Lot ID Number | Map File Name |
|-----------------------------|----------------|---------------|---------------|
| ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ | T0000 | Lot 123 | Lot123.T0000 |
| ● ● ● ● ● ● ● ● ● ● ● ● ● ● | T4095 | Lot 456 | Lot456.T4095 |
| ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ● | T0001 | Lot 100 | Lot100.T0001 |
| ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ● ● | T0003 | Lot 100 | Lot100.T003 |
| ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ● ○ | T0002 | Lot 000 | Lot100.T002 |

Now returning to FIG. 7, after a first map 122 and a second map 124 are created from the results of two different test steps, the corresponding test results, recorded in both maps 122 and 124, are combined to generate a final sorting map using a linked algorithm. The off-line sorting process begins by the sorting unit receiving these composite test results from the final sorting map. For example, when the room/cold (or ambient) test is performed first and the hot sort test is performed later, the corresponding map files are named "Lotxxx.TxxxxA" and "Lotxxx.TxxxxH," respectively (where xxx represents the lot ID number, "T" indicates a test tray, xxxx represents the tray ID number, "A" designates the ambient test, and "H" designates the hot sort test). The final sorting map is stored in a final composite map file named "Lotxxx.TyyyS" (where yyy represents the number of test trays in one lot and "S" indicates a sorting map).

A similar naming scheme can be employed in the rework (retest) process, where the final sorting map file name is associated with a name of the retest composite map files.

Each of the test maps 120 according to this embodiment has eight rows and eight columns, forming sixty-four cells, and corresponds to a respective one of the test trays, in which sixty-four devices are stored. Furthermore, the maps 122 and 124 separately contain the test results from two different test and burn-in apparatuses. In this example, one sheaf (or subgroup) of the maps 122 or 124 consists of four individual maps corresponding to the four test heads in one of the test and burn-in apparatuses. Test result numerals entered in the map represent corresponding testing results or information obtained regarding the device at that location in the test tray. Specifically, the meaning of the test result numerals is as follows: a "φ" stands for socket-off, a "1-3" represents good devices, a "4-7" indicates failed devices, an "8" stands for open/short, and a "21" indicates a soft bin device (or special fail bin device) for a specified customer. A cell formed by any column and any row in the first map 122 will be designated below "(C, R)I," while a cell in the second map 124 will be designated "(C, R)II" (where "C" stands for the column number, "R" stands for the row number, and "I" and "II" are the map numbers corresponding to their respective tests). Thus, the test results corresponding to a single device are recorded at the same position in each of the test tray maps 120. The annotations in parentheses on the second map 124 indicate sorting commands (i.e., "1-3", "R₁", "R₂", "R₃", "BGD", "T_{III}", and "Bonus") according to the composite map results obtained by combining the first map 122 and the second map 124 into the final sorting map for off-line sorting. The final sorting map can normally be created by a link map algorithm which combines the test results for a given device from multiple test tray maps.

The sorting step utilizes the test tray maps 120 and is carried out by means of a test program which sorts the devices according to their tested characteristics. If the test result numeral of any cell (C, R)I in the first map 122 equals that of the corresponding cell (C, R)II in the second map 124, the test program is able to come to a definite decision regarding the state of the device corresponding to that cell location based on the test result numeral. Specifically, when the test result numeral in corresponding cells, i.e., (3, 5)I and (3, 5)II, in both the first and second map 122 and 124, respectively, is a "1", the device corresponding to that cell location (i.e., the third column and fifth row of the test tray) is confirmed to be a good device. A conclusion that the device is good is represented by the sorting command "1", "2" or "3", as shown in parentheses in the second map 124. Additionally, when the test result numeral in corresponding cells, i.e., (4, 2)I and (4, 2)II, is an "8", the corresponding device is determined to be opened/shorted and will therefore be scrapped during a sorting process. Similarly, when the test result numeral is a "4" in both cells, i.e., (5, 3)I and (5, 3)II, when the test result numeral is a "5" in both cells, i.e., (5, 6)I and (5, 6)II, or when the test result numeral is a "6" in both cells, i.e., (7, 3)I and (7, 3)II or (8, 3)I and (8, 3)II, the corresponding device is also determined to be a failed device and will be scrapped. The conclusion that the device is a failed device is represented by the sorting command "R₃" in parentheses in the second map 124.

On the other hand, if the test result numeral of any cell (C, R)I in the first map 122 differs from that of the corresponding cell (C, R)II in the second map 124, then the test program comes either to a decision to retest the corresponding device by a particular test, to a conclusion that it is a good device,

to a conclusion that it is a failed device, or to a decision to classify the device as bin grade down (BGD), as is well known in the art. A decision to retest the device by the first test may be made when the test result numeral in the first map indicates a failed or open/shorted device but the test result numeral in the second map indicates a good device. For example, when the test result numeral in a cell in the first map, i.e., (5, 1)I, is a "5", indicating failure of the first test, but the test result numeral in the corresponding cell of the second map, i.e., (5, 1)II is a "3", passing the second test, the program concludes that the device should be retested by the first test. A decision to retest by the first test is designated by the sorting command "R₁". Similarly, when the test result numeral in a first map cell, i.e., (2, 1)I, is a "φ", which stands for socket-off, while in the corresponding cell of the second map, i.e., (2, 1)II, it is a "2", indicating a good device, the corresponding device will be also be retested by the first test.

A decision to retest by the second test is reached in a similar way. For example, if the test result numeral in a first map cell, i.e., (6, 5)I, is a "1" but the test result numeral in the corresponding cell, i.e., (6, 5)II, of the second map 124 is an "8", then the corresponding device will be retested by the second test. Similarly, if the first map cell and corresponding second map cell contain a "1" and a "φ", respectively (i.e., (3, 8)I and II), the decision will be made to retest the device by the second test. This decision to retest by the second test is designated by the sorting command "R₂".

When the test result numeral found in a first map cell is a "21," i.e., cell (1, 3)I, indicating a special fail bin for a specified customer under the first test, if the device corresponding to that cell location performs satisfactorily enough under a second test to receive a good test result numeral, i.e. a "2" in cell (1, 3)II, then that device will be sorted as a good device to any customers other than the specified customer. This decision is designated by the sort command "T_{III}" in the final sorting map. The device will be sorted as bin grade down (BGD) and given the sort command "BGD" when the test result numeral in a cell of one map, i.e., (6, 1)I, is a "5", indicating a failed device, but the test result numeral in a corresponding cell, i.e., (6, 1)II, is a "2", indicating a good device.

Bin numbers are normally divided in to two groups, one for good devices, the other for bad devices. Devices in a good bin are also divided in to different grades based on device speed, power consumption, and so on. Here, bin1, bin2, and bin3 represent good bins. In general, the numerals 1-8 represent a degree of desirability, e.g., bin2 represents a less desirable device (slower speed, more power consumption) than a "1".

R1, R2, and R3 are decided by a test engineer based on a combination of test steps (hot/cold) and pass/fail. Some possible combinations of 1-8 for R1, R2, and R3 are shown in Table 1A:

TABLE 1A

| Hot (or Cold) | Hot (or Cold) | |
|----------------------|----------------------|----|
| Pass (1, 2, 3) | Fail (4, 5, 6, 7, 8) | R2 |
| Fail (4, 5, 6, 7, 8) | Pass (1, 2, 3) | R1 |
| Fail (4, 5, 6, 7, 8) | Fail (4, 5, 6, 7, 8) | R3 |

Unlike the prior art retest process, which is performed repeatedly using the same tester and handler after each of the several sorting steps, the retest process of the present invention is performed on retest designated devices following the composite sorting process. Alternatively, the retest process

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of the present invention can be performed all at one time for each of the various kinds of failed devices (i.e., "R₁," "R₂" and "R₃" devices). In this embodiment, the retest devices are shifted into the device trays during the sorting step so they can be retested. They are then loaded into retest trays and, after the testing process of one lot is finished, they are transported to the first test and burn-in apparatus. The retest trays are the same shape as the test trays, but preferably have a different color to facilitate distinction between the two types of trays. The previous test results corresponding to the failed devices are not discarded but are instead retained for complete compilation with the new test results. Therefore, the "R₁," "R₂" and "R₃" designations are retained throughout the retest process.

When the retest tray is supplied to the in-line system, the entire test process is repeated for each of the retest devices regardless of their particular type of fail. The retest map files are named Lotxxx.Rxxxx, Lotxxx.RxxxxA, Lotxxx.RxxxxH, and Lotxxx.RzzzS (where "zzz" represents the number of retest trays in one lot and "R" indicates retest maps). Once a final retest sorting map file Lotxxx.RzzzS is generated, the two final map files Lotxxx.TyyyS and Lotxxx.RzzzS are automatically combined into a cumulative map file named Lotxxx.F***S (where * equals y plus z) and also stored as a test data file Lotxxx.F***F. This test data file contains twice the amount of test information as the non-retest final sorting map files, and includes cumulative yield data. This enables the retest devices to be evaluated and sorted based on the cumulative results obtained from the combination of the initial testing process results and the retest results.

FIG. 8 is a schematic view of a second preferred embodiment of the test and burn-in (TABI) apparatus 300 in accordance with the present invention. As shown in FIG. 8, the TABI apparatus 300 has nearly the same structure as the TABI apparatus 100 according to the first preferred embodiment shown in FIG. 4. Unlike the previous embodiment, however, eight test heads 23 are provided rather than four. Additionally, there are two main frames 21, and two chambers 32 provided for each apparatus. Furthermore, the positions of both a loader 134 and an unloader 136 also differ from the previous embodiment. More specifically, the loader 134 and the unloader 136 are formed at the upper and lower parts of one end of the rail 38. For convenience of reference, the loader 134 and unloader 136 in FIG. 8 are illustrated side by side, however, they are actually stacked. Therefore, the rail 38 in the chamber 32 is formed having double layers, each layer of which is connected to either the loader 134 or the unloader 136. Reference numeral 140 represents the moving direction of the test trays (new trays 10a or tested trays 10b) in the double-layered rail 38. The positions of the loader 134 and the unloader 136 can be changed.

An in-line system 400 which employs the TABI apparatus 300 of the second preferred embodiment, as shown in FIG. 8, is schematically depicted in FIG. 9. As seen from FIG. 9, the in-line system 400 of the back-end process includes three sub-in-line systems each of which are composed of three TABI apparatuses 300a, 300b and 300c, and one sorting unit 351, standing in a row. Test processes can proceed independently in each sub-in-line system.

The in-line system 400 further includes a transferring member 40 which goes from and returns to the same side of the test apparatuses due to the similar positioning of their loaders and unloaders. The sorting unit 351 is made up of double units. The in-line system 400 of this embodiment can be maximized through appropriate modification of the configuration of several units including the sorting unit, namely,

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by adjusting throughput of all apparatuses and units. Reference numerals 355 and 356 in the sorting unit 351 refer to the unloading part of the tested devices and the loading part of new devices. The operation of these elements is similar to that of the first preferred embodiment described with reference to FIG. 5 and a redundant description here is therefore omitted.

As previously described, the prior art burn-in tester of JEC Co. is not able to perform several test items with a short cycle such as pattern sensitivity, Vcc margin, refresh, or speed sorting. Therefore, the room/cold test and the hot sort test have been carried out separately from the burn-in process. Remarkably, the TABI apparatus and the in-line system of this invention permit the room/cold test, the hot sort test, and the burn-in process to all be performed with the same platform. One of the reasons why this improvement is possible is that the test rate of the burn-in process can be improved up to the order of that of the room/cold test or the hot sort test. This improvement also enables the employment of test trays instead of the burn-in board. In particular, in the embodiment where the Schlumberger Co. tester is used, it is possible to perform the testing of test items requiring a shorter cycle such as a 200 MHz test rate and a 1 ns transition time. Moreover, the present invention can reduce the cycle period in the burn-in process as shown in Tables 2 and 3.

TABLE 2

Information List of Conventional Burn-in

| Device | Burn-In Time (hours) | Vcc (V) | Temperature (° C.) | Cycle Period (ns) |
|---------------|----------------------|---------|--------------------|-------------------|
| 16M DRAM | 2 | 5.5 | 125 | 500 |
| 64M DRAM | 12 | 6.3 | 125 | 2000 |
| 16M Sync DRAM | 2 | 5.5 | 125 | 900 |
| 64M Sync DRAM | 12 | 5.5 | 125 | 900 |
| 1M Sync SRAM | 2 | 5.5 | 125 | 1000 |
| 2M Sync SRAM | 2 | 5.5 | 125 | 1000 |

TABLE 3

Information List of Invented Burn-in

| Device | Burn-In Time (sec) | Vcc (V) | Temperature (° C.) | Cycle Period (ns) | The Rate of Reduction |
|---------------|--------------------|---------|--------------------|-------------------|-----------------------|
| 16M DRAM | 600 | 5.5 | 125 | 90 | 1/5.5 |
| 64M DRAM | 360 | 6.3 | 125 | 90 | 1/22 |
| 16M Sync DRAM | 240 | 5.5 | 125 | 30 | 1/30 |
| 64M Sync DRAM | 1440 | 5.5 | 125 | 30 | 1/30 |
| 1M Sync SRAM | 72 | 5.5 | 125 | 10 | 1/100 |
| 2M Sync SRAM | 72 | 5.5 | 125 | 10 | 1/100 |

Tables 2 and 3 set forth only the burn-in time itself at 125° C. Accordingly, if incidental time such as the time taken in performing the sorting step were also to be considered, the actual processing time of the conventional burn-in of Table 2 would be much longer. Contrary to this, the actual process time of the burn-in process of the present invention as disclosed in Table 3 is not as drastically different from the burn-in time itself as is the actual processing time of the prior art, since there is only one sorting step and transfer between trays is unnecessary.

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As described so far, the test and burn-in apparatus, the in-line system and the method according to the present invention produce excellent outcomes in the back-end process for the manufacture of semiconductor devices. Namely, an apparatus and system are provided which occupy much less space, offer a shorter turn around time (TAT), provide for a reduction of movement, reduce the tester and handler cost, improve yield and quality, reduce manpower requirements for maintenance and operation, allow for the removal of human error, improve the work in process (WIP), allow part-to-part failure analysis by data tracking and comparisons, provide accurate data feedback to other divisions, and so on.

A test and burn-in apparatus for semiconductor chip package devices, an in-line system which includes the test and burn-in apparatus, and a test method which employs the in-line system are provided. A test and burn-in apparatus for testing semiconductor devices allows various testing processes, including a burn-in process, to be performed at the same testing stage. The apparatus employs test trays which contain the semiconductor devices. These test trays are used throughout the in-line system so that an entire back-end process can be performed without the need for loading/unloading the semiconductor devices into and from device trays between the various tests. The test and burn-in apparatus according to this invention can therefore occupy less space than the prior art testing apparatuses. The in-line system includes multiple test and burn-in apparatuses as well as a single sorting unit which performs a composite sorting operation after all the testing processes have been performed. Furthermore, the method for testing the semiconductor devices in the in-line system includes testing the semiconductor devices in the test trays using the test and burn-in apparatus, generating a test tray map corresponding to results of the test, transferring the test trays to a different testing apparatus for a second testing and test tray map generation process, and finally sorting the semiconductor devices in the sorting unit after all testing processes have been performed based on a final sorting map created by combining the test tray maps of each of the tests. The benefits of this invention are reduced time and space requirements because neither transferring the devices to device trays between tests nor performing multiple sorting steps are required.

Throughout the drawings and specification, preferred embodiments of the present invention have been disclosed which, although specific terms are employed, are used merely in a generic and descriptive sense and should not be considered as limiting in any way the spirit and scope of the invention as set forth in the following claims.

What is claimed is:

1. An in-line system, comprising:

a plurality of test and burn-in apparatuses, each test and burn-in apparatus configured to perform one of a plurality of test and burn-in processes, different from the test and/or burn-in processes performed by the other test and burn-in apparatuses, wherein each test and burn-in apparatus comprises a rail for transporting a plurality of test trays, each test tray configured to contain a plurality of semiconductor devices, a loader for loading the test trays onto the rail, an unloader for unloading the test trays from the rail, a chamber through which the rail traverses, so that the semiconductor devices contained in the test trays loaded onto the rail can be subjected to a test and burn-in process within the chamber, and a plurality of test heads associated with the chamber, wherein each test head is

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electrically connected to a corresponding test tray within the chamber in order to perform the test and burn-in process;

a transferring member configured to transfer the test trays between the test and burn-in apparatuses, wherein the transferring member receives the test trays from the unloader of one of the test and burn-in apparatuses and supplies the test trays to the loader of another one of the test and burn-in apparatuses, whereby the apparatuses are linked together in-line by the transferring member; and

a sorting unit configured to sort the semiconductor devices based on a result of the test and burn-in processes and also configured to deliver the semiconductor devices to a device tray from the test trays.

2. The in-line system according to claim 1, wherein each of the test burn-in apparatuses further comprises a main frame comprising a control unit which is capable of being electrically connected to the test heads.

3. The in-line system according to claim 2, wherein the control unit of each of the test and burn-in apparatuses is electrically connected to the sorting unit.

4. The in-line system according to claim 2, wherein each of the main frames further comprises a coolant refrigerator unit configured to cool down the test heads.

5. The in-line system according to claim 1, wherein the plurality of test and burn-in apparatuses comprise a first apparatus configured to perform a DC test and a burn-in process, a second apparatus configured to perform a room/cold test, and a third apparatus configured to perform a hot sort test.

6. The in-line system according to claim 1, wherein the sorting unit is configured to perform two operations, namely, moving tested devices from the test trays to the device tray, and providing new devices from a new device tray to the test trays.

7. The in-line system according to claim 1, wherein the sorting unit is in communication with a marking unit and a visual inspection unit further processing of the tested devices in the device tray.

8. A method for testing semiconductor devices, comprising:

providing a plurality of test trays to a first test and burn-in apparatus, wherein each test tray is configured to receive a plurality of semiconductor devices;

testing the semiconductor devices in the test trays in a first test and burn-in apparatus;

automatically transferring the test trays from the first test and burn-in apparatus to a second test and burn-in apparatus;

testing the semiconductor devices in the test trays in the second test and burn-in apparatus;

automatically transferring the test trays from the second apparatus to a third test and burn-in apparatus;

testing the semiconductor devices in the test trays in the third test and burn-in apparatus;

automatically transferring the test trays from the third test and burn-in apparatus to a sorting unit; and

sorting the semiconductor devices in the test trays.

9. The method according to claim 8, wherein automatically transferring the test trays comprises receiving the test trays from an unloader of one of the test and burn-in apparatuses and supplying the test trays to a loader of another one of the test and burn-in apparatuses.

10. The method to claim 9, wherein sorting the semiconductor devices comprises transmitting a plurality of test tray

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maps to a sorting unit via the control units of the test and burn-in apparatuses and sorting the semiconductor devices in the sorting unit based on the test tray maps.

11. The method according to claim 8, further comprising: loading new semiconductor devices contained in new device trays to the test trays, and then providing the test trays to the first test and burn-in apparatus.

12. The method according to claim 8, wherein testing in each of the first, second and third test and burn-in apparatuses comprises performing a test and/or burn-in process selected from a group consisting of a burn-in process, a room/cold test, and a hot sort test.

13. An apparatus for performing a back-end process, comprising:

a host computer;

a test tray configured to receive a plurality of semiconductor devices;

a test head configured to communicate with the semiconductor devices in the test tray and the host computer; and

a transferring member configured to receive the test tray and to transport the test tray into alignment with the test head so that a test can be performed on the semiconductor devices by the test head, wherein mapping signals are sent from the test head to the host computer for processing after the test is performed.

14. The apparatus as recited in claim 13 wherein the host computer is configured to process the mapping signals to create a test tray map which comprises test results and other information obtained from the test performed on the devices.

15. The apparatus as recited in claim 13, wherein the test tray comprises a plurality of holes representing a tray ID number which can be used to automatically generate map file names for storing the test tray maps in the host computer.

16. The apparatus as recited in claim 13, further comprising:

a sorting unit in communication with the host computer, the sorting unit being configured to receive a final sorting map from the host computer.

17. The apparatus as recited in claim 16, wherein the apparatus further comprises a plurality of device trays and wherein the sorting unit is configured to move tested devices, comprising good devices and failed devices, from the test tray to the device trays in response to data contained in the final sorting map.

18. The apparatus as recited in claim 17 wherein the apparatus further comprises a retest tray and wherein the sorting unit is further configured to move the failed devices from a device tray containing failed devices to the retest tray, or configured to move new devices from new device trays to the test tray.

19. The apparatus as recited in claim 17, further comprising:

a marking unit and a visual inspection unit linked to the sorting unit, wherein a device tray containing good devices is transferred to the marking unit and the visual inspection unit.

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20. A method for testing semiconductor devices performed on an apparatus including a host computer, a plurality of test trays being configured to hold a plurality of semiconductor devices and a plurality of test heads being configured to make electrical connection with the semiconductor devices when they are held by one of the test trays, the test heads being configured to be in communication with the host computer via network system, the method comprising:

automatically transporting the plurality of test trays for alignment with the test heads;

testing devices using the test heads; and

sending mapping signals to the host computer, the mapping signals providing data for processing results of the testing devices by the test heads.

21. The method according to claim 20, further comprising:

processing the mapping signals into test tray maps representing the devices in the trays in order to identify the results of the tests performed on the devices by the test heads.

22. The method as recited in claim 21 wherein each of the test trays comprises a plurality of holes to identify a tray ID number, and wherein the method further comprises:

recognizing the tray ID number by sensing the holes of each test tray; and

generating a file name of each map file from a combination of the tray ID number and a lot ID number.

23. The method as recited in claim 22 wherein testing includes performing a plurality of different types of tests, each test head being capable of performing one of the tests, and wherein a plurality of test tray maps representing the different types of tests are distinguished from the others using file names having a predetermined format.

24. A method according to claim 23 further comprising:

receiving signals representing a final sorting map into a sorting unit from the host computer, wherein the final sorting map is created by automatically combining the maps representing the different types of tests;

moving the tested devices, which include good devices and failed devices, from the test trays to a device tray in response to the final sorting map.

25. The method according to claim 24, further comprising:

moving the failed devices from the device tray to a retest tray using the sorting unit.

26. The method as recited in claim 25, further comprising: automatically transporting the retest tray for alignment with the test heads so that the test heads can perform a retest on the failed devices; and

sending mapping signals to the host computer, the mapping signals providing data for processing the results of the retest performed on the failed devices by the test heads.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,563,331 B1
DATED : May 13, 2003
INVENTOR(S) : Ju-Seok Maeng

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4,

Line 17, "burn in processes" should read -- burn-in processes --.

Column 12,

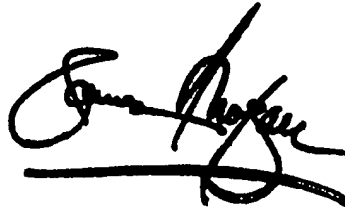
Table 1, "Lot 000" should read -- Lot 100 --.

Column 13,

Line 46, "is a "I" should read -- is a "1" --.

Signed and Sealed this

Second Day of December, 2003

A handwritten signature in black ink, appearing to read "James E. Rogan", with a horizontal line drawn underneath it.

JAMES E. ROGAN
Director of the United States Patent and Trademark Office



US006507206B1

(12) **United States Patent**
Vesaruch et al.

(10) **Patent No.:** **US 6,507,206 B1**
(45) **Date of Patent:** **Jan. 14, 2003**

(54) **AUTOMATED PREVENTION OF TRANSFER OF AN UNSOAKED IC PACKAGE FROM A TEMPERATURE SOAKING CHAMBER TO A TESTING CHAMBER**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 296 days.

(21) Appl. No.: **09/690,080**

(22) Filed: **Oct. 16, 2000**

(51) Int. Cl.⁷ **G01R 31/02**

(52) U.S. Cl. **324/760; 324/158.1; 324/765**

(58) Field of Search **324/158.1, 760, 324/765; 209/573; 221/12, 15, 83**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,588,092 A * 5/1986 Moechnig et al. 324/158.1
4,926,118 A * 5/1990 O'Connor et al. 209/573
5,261,775 A * 11/1993 Kobayashi 324/158.1
5,307,011 A 4/1994 Tani 324/158.1

FOREIGN PATENT DOCUMENTS

WO 92/04989 4/1992 G01R/31/28

* cited by examiner

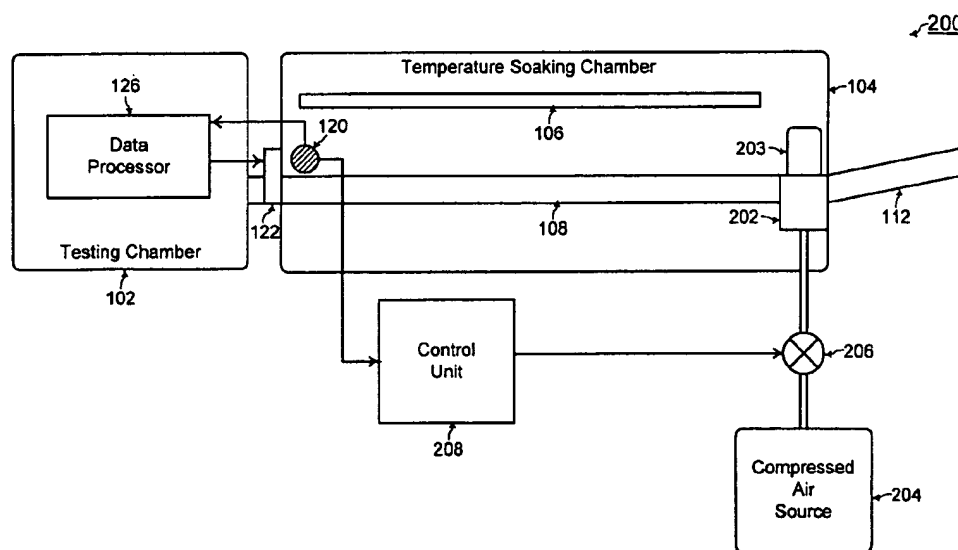
Primary Examiner—Ernest Karlsen

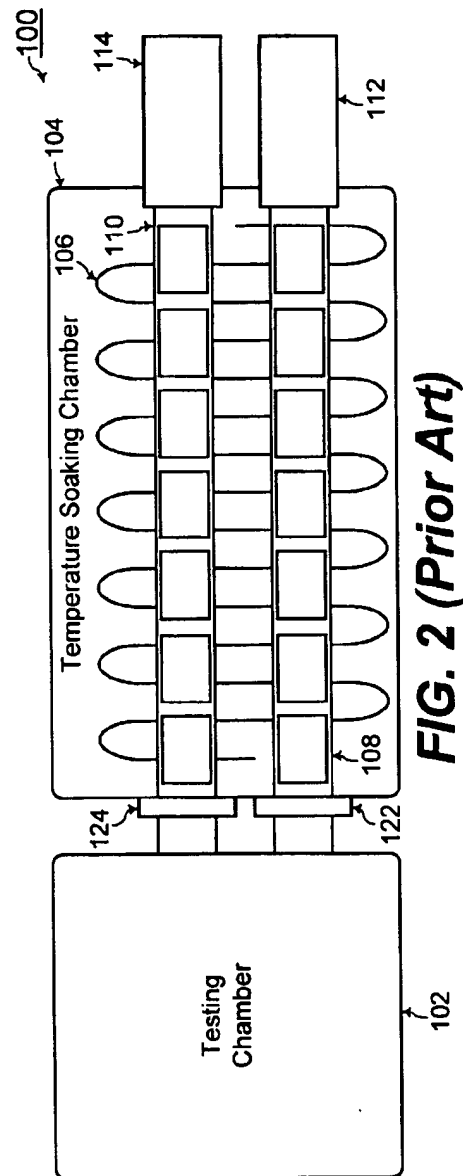
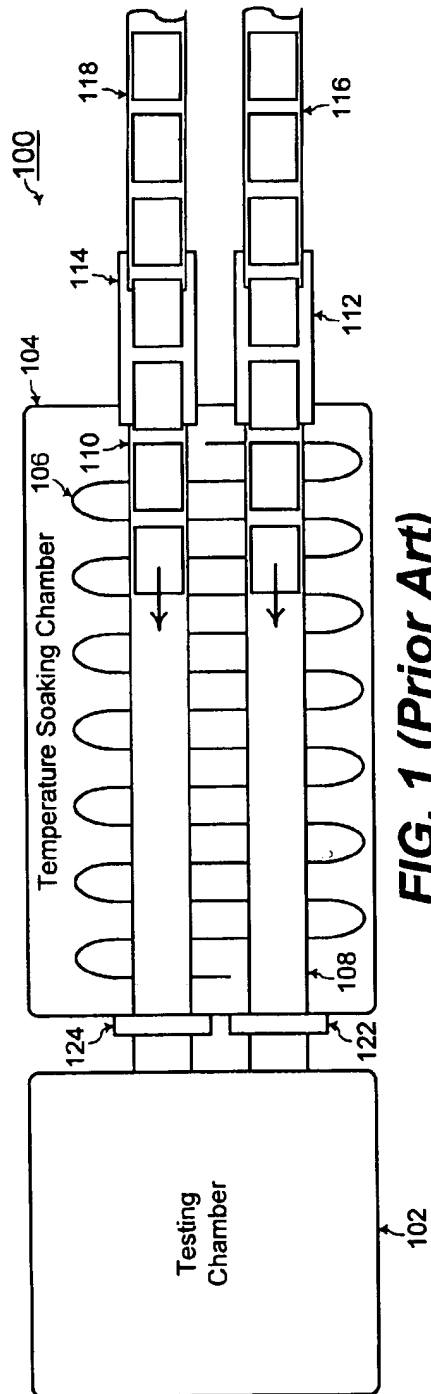
(74) *Attorney, Agent, or Firm*—Monica H. Choi

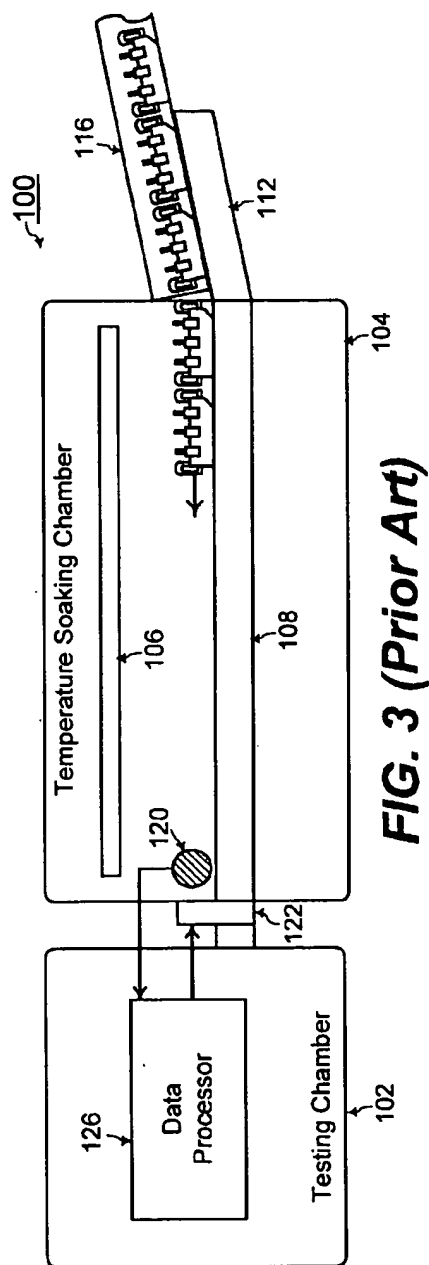
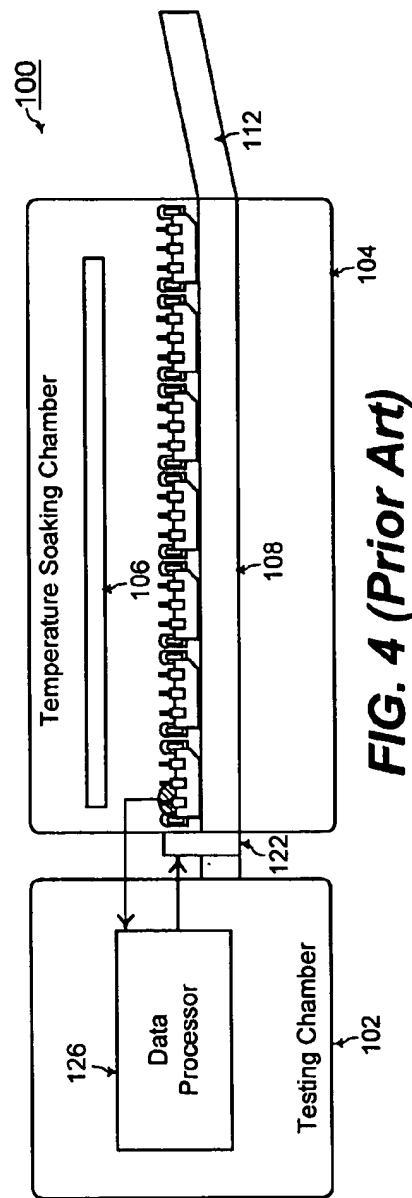
(57) **ABSTRACT**

For ensuring that each of a plurality of IC (integrated circuit) packages are placed within a temperature soaking chamber for a predetermined time period before being transferred to a testing chamber, an input stopper device is disposed at an input of a track with the track being disposed through the temperature soaking chamber. A prior container holding a prior plurality of IC packages is placed at the input of the track such that the prior plurality of IC packages slides out of the prior container along the track into the soaking chamber when the input stopper device is at a passing position. The prior plurality of IC packages is placed within the soaking chamber for the predetermined time period before each of the prior plurality of IC packages is transferred to the testing chamber when an output stopper device at an output of the track within the soaking chamber is placed to a passing position. A control unit, coupled to the input stopper device, controls the input stopper device to be at a stopping position until each of the prior plurality of IC packages has been transferred to the testing chamber and until the output stopper device is placed to a stopping position when the control unit controls the input stopper device to be at the passing position. Thus, each of a subsequent plurality of IC packages within a subsequent container is blocked, by the input stopper device, to be contained within the subsequent container placed at the input of the track until each of the prior plurality of IC packages within the soaking chamber has been transferred to the testing chamber. In addition, each of the subsequent plurality of IC packages is blocked by the output stopper device from being transferred to the testing chamber until the subsequent plurality of IC packages has been within the soaking chamber for the predetermined time period.

15 Claims, 10 Drawing Sheets





**FIG. 3 (Prior Art)****FIG. 4 (Prior Art)**

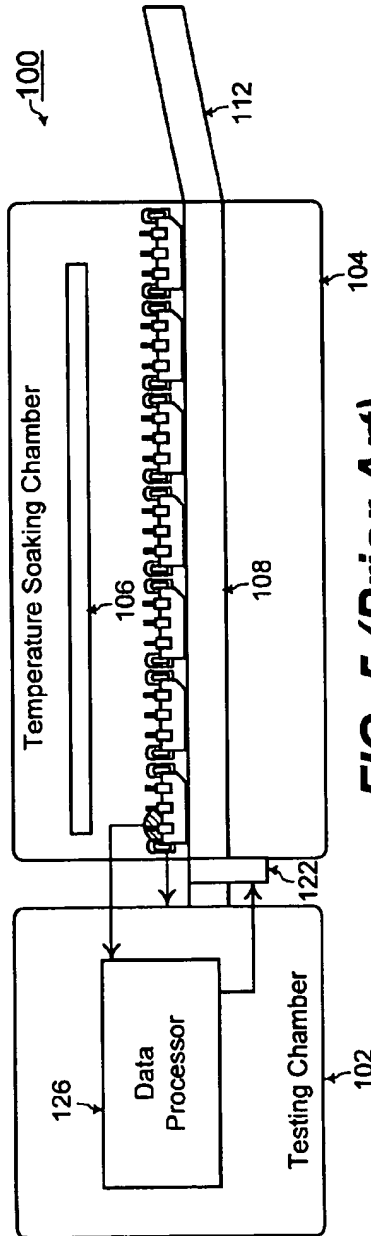


FIG. 5 (Prior Art)

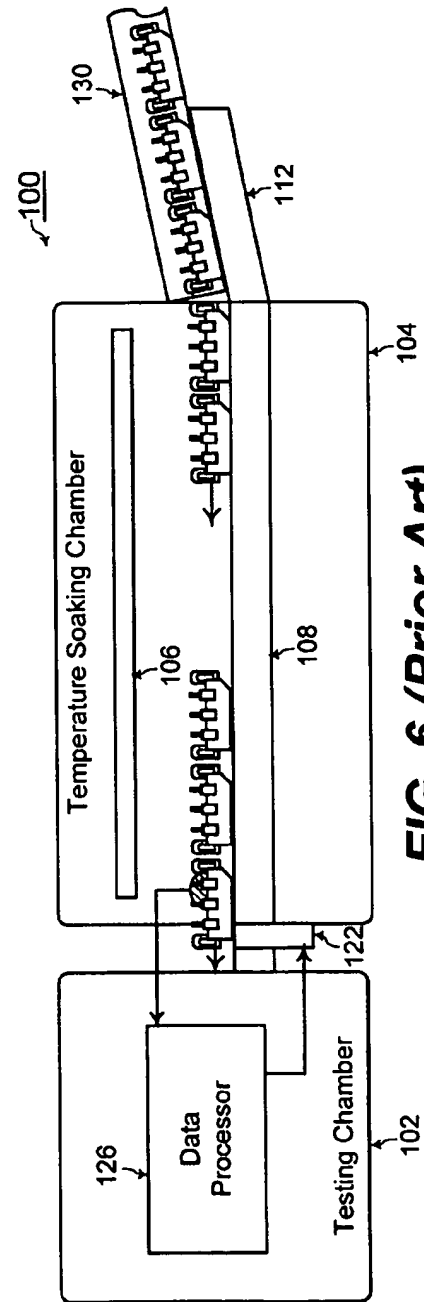


FIG. 6 (Prior Art)

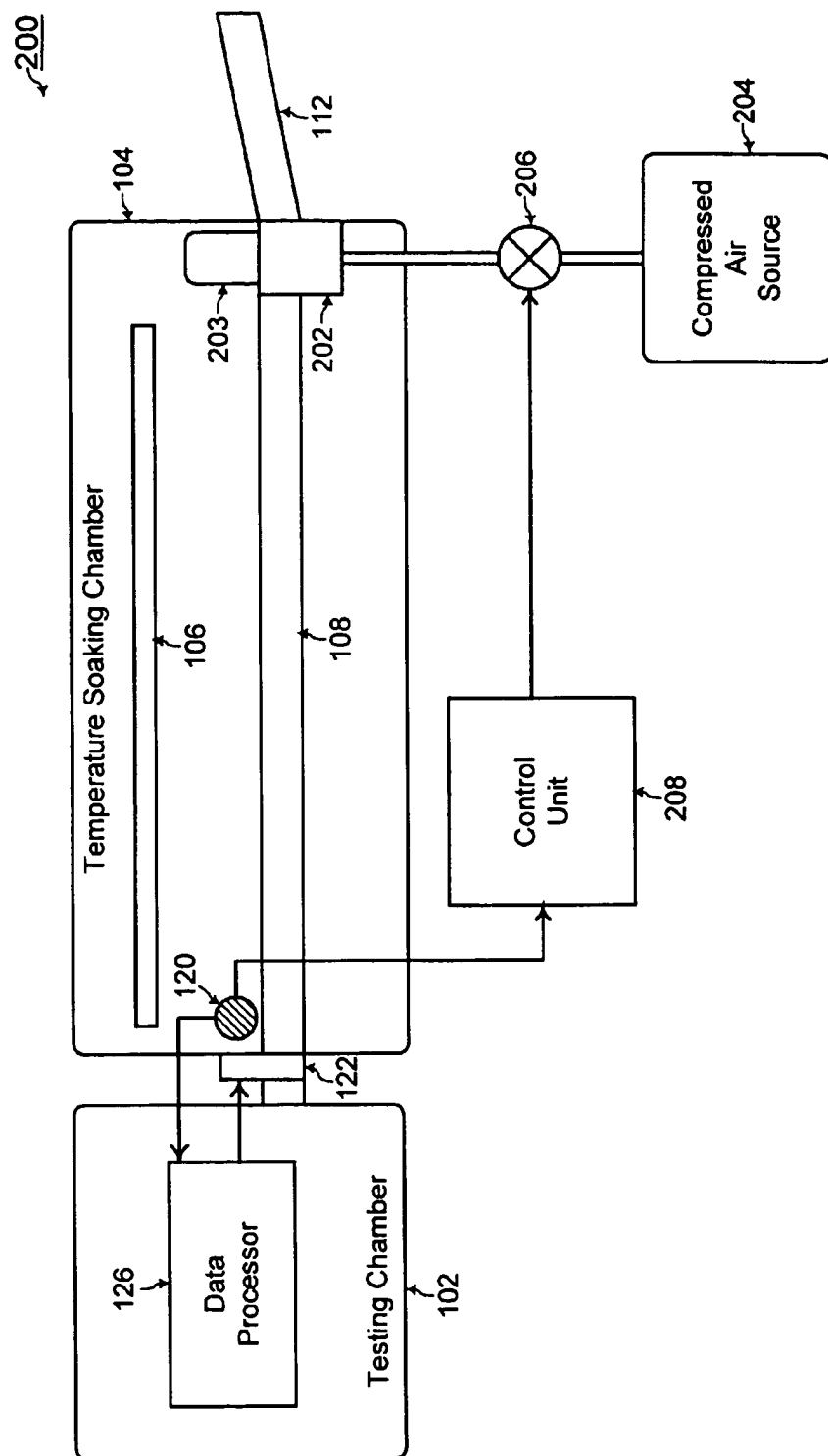
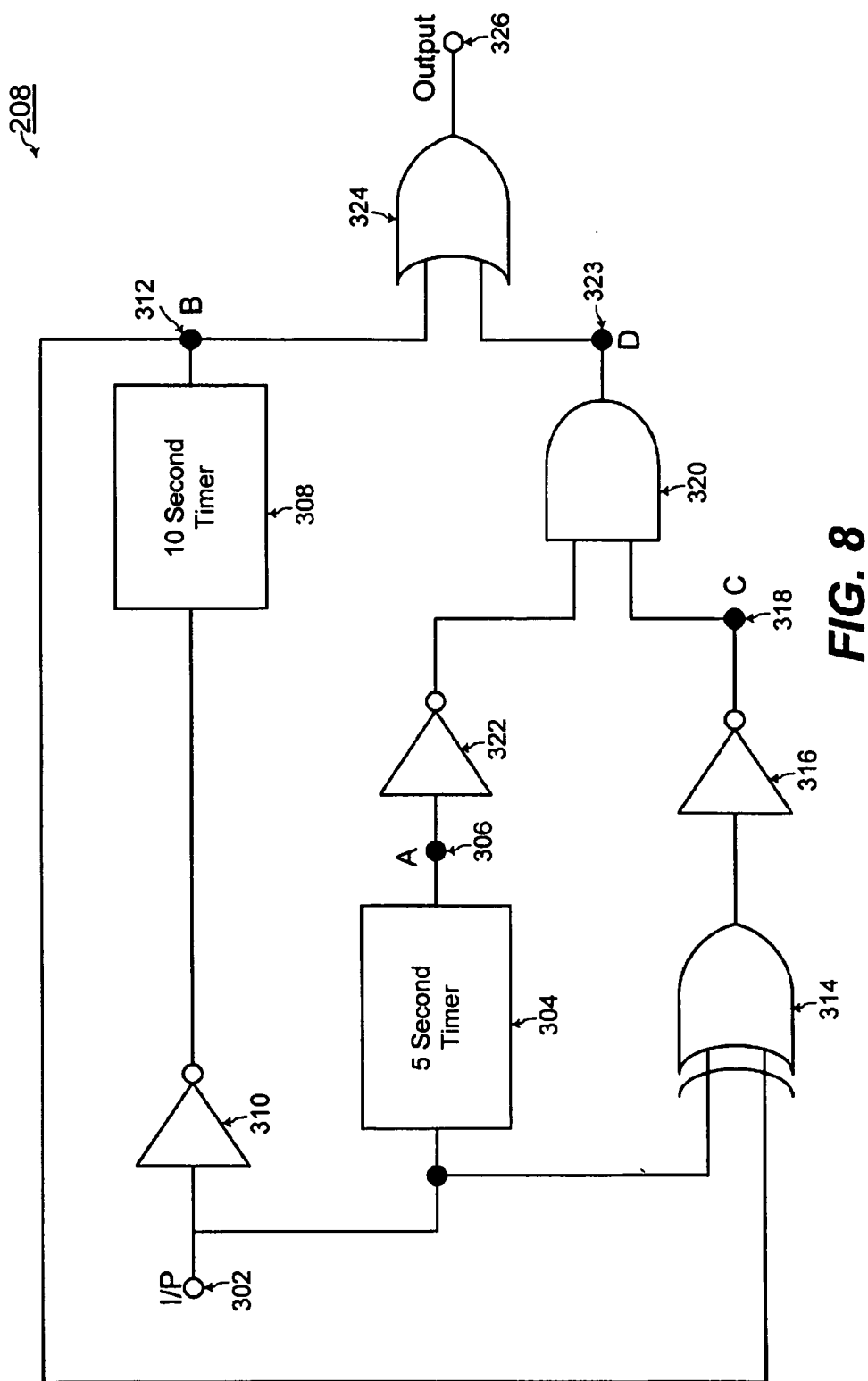


FIG. 7



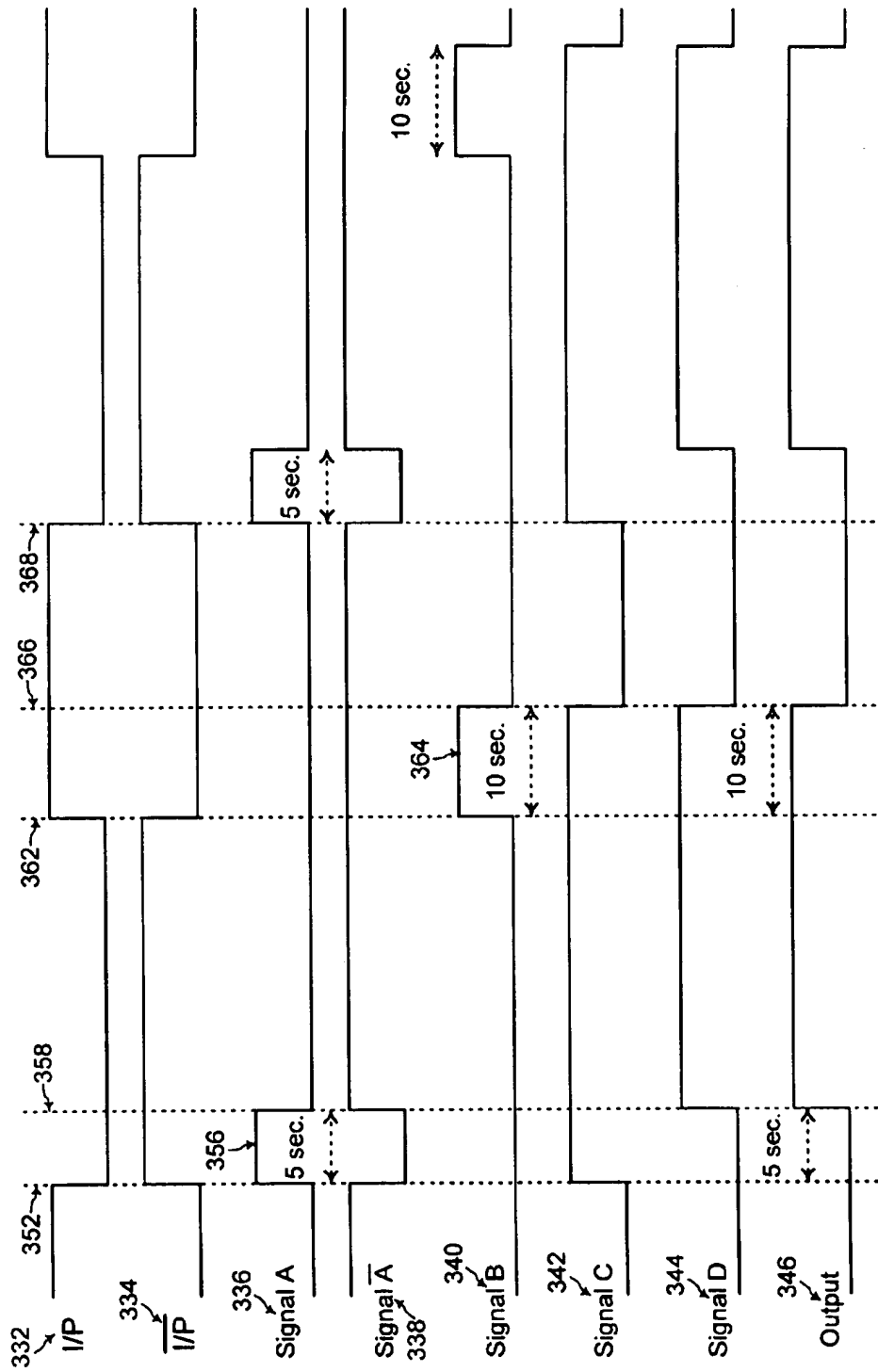
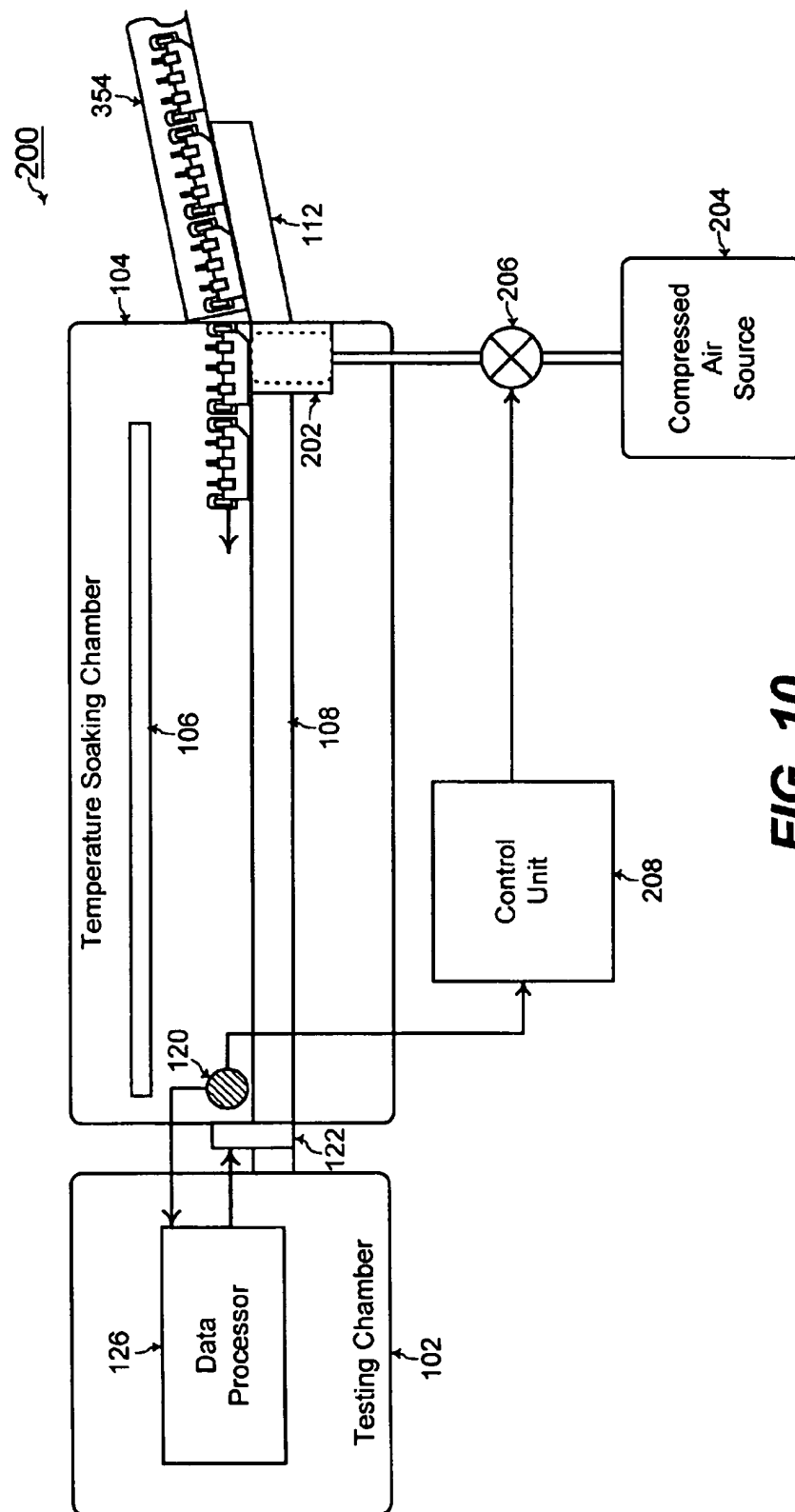


FIG. 9

**FIG. 10**

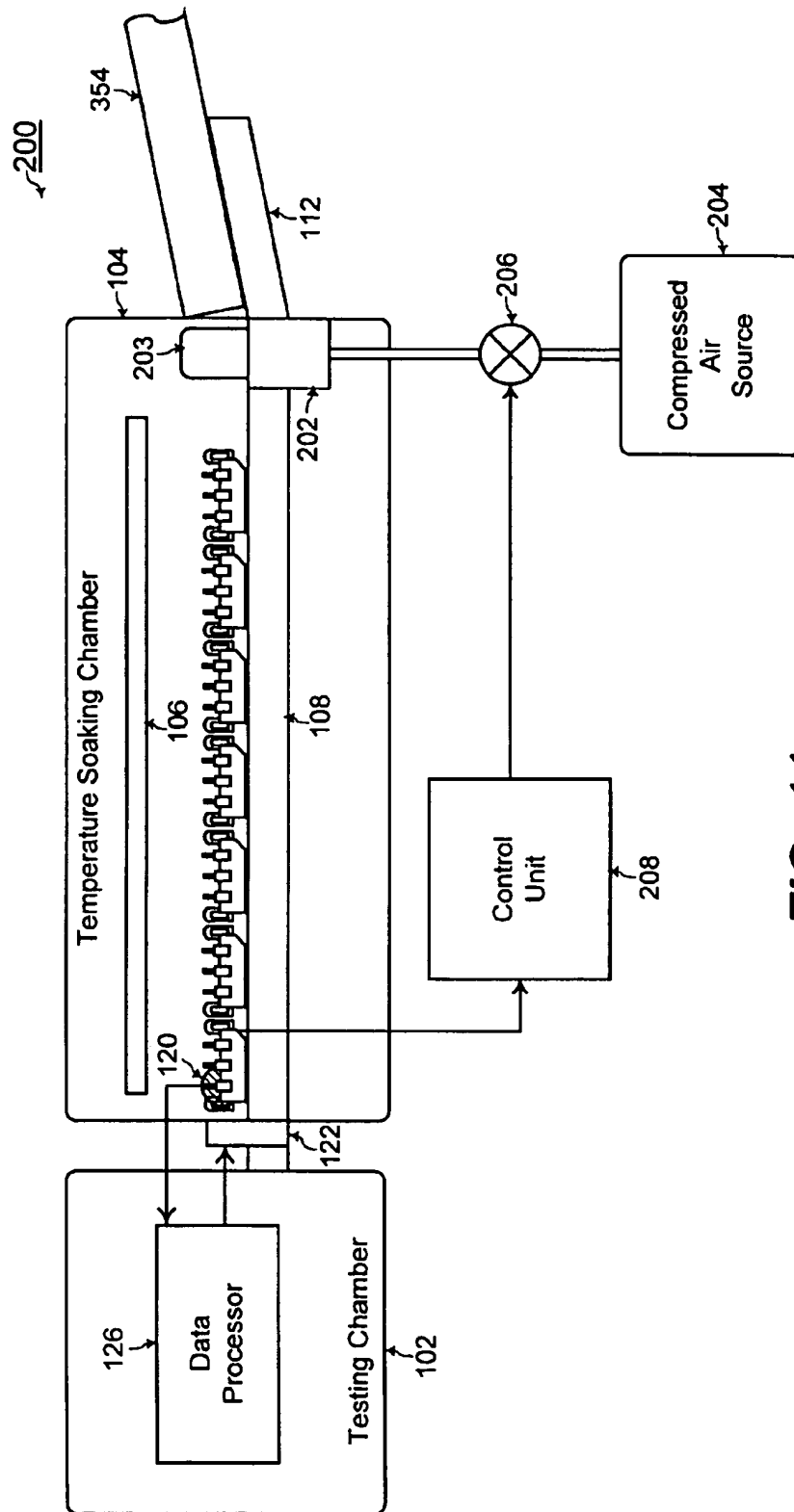
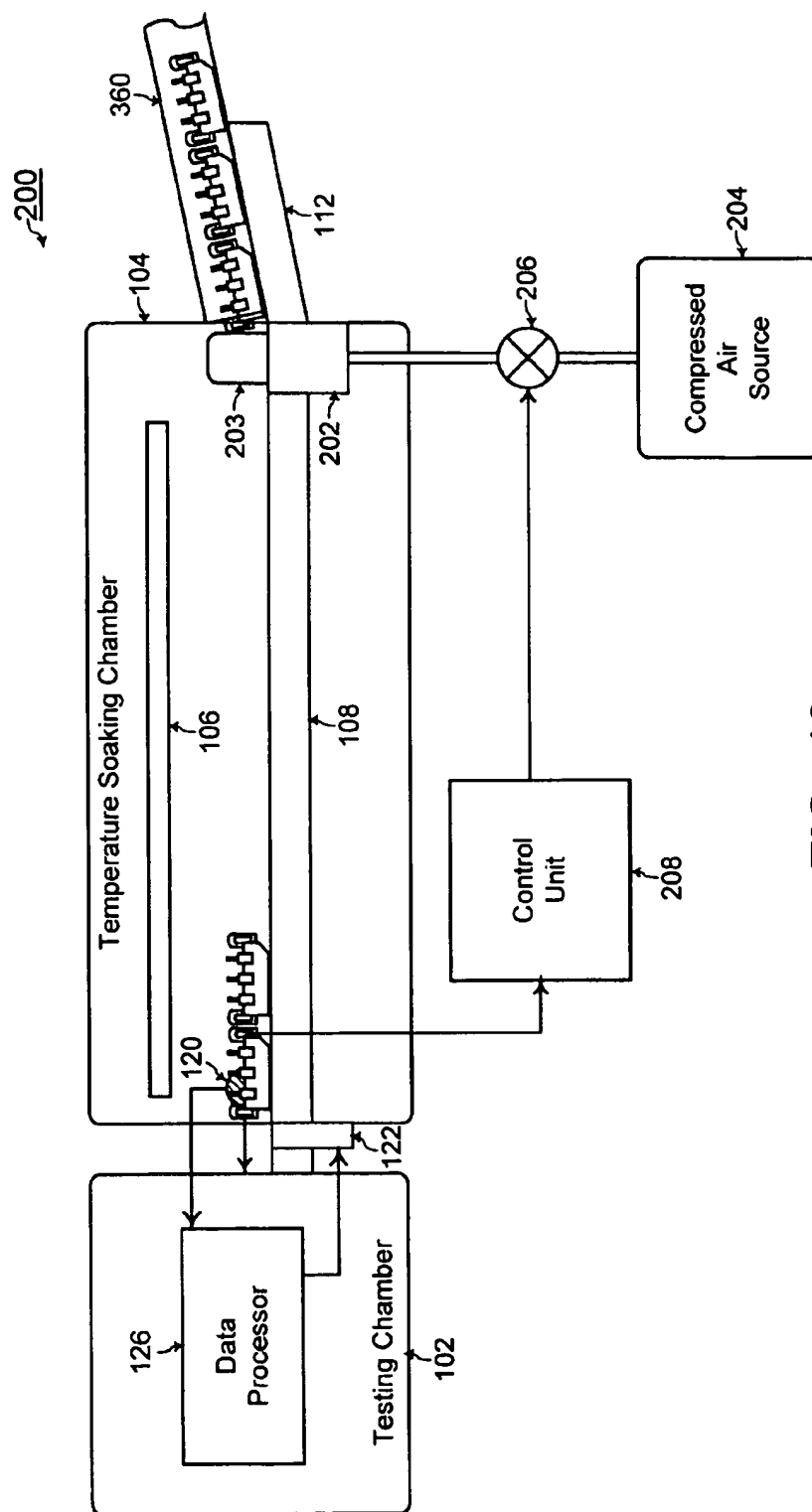


FIG. 11

**FIG. 12**

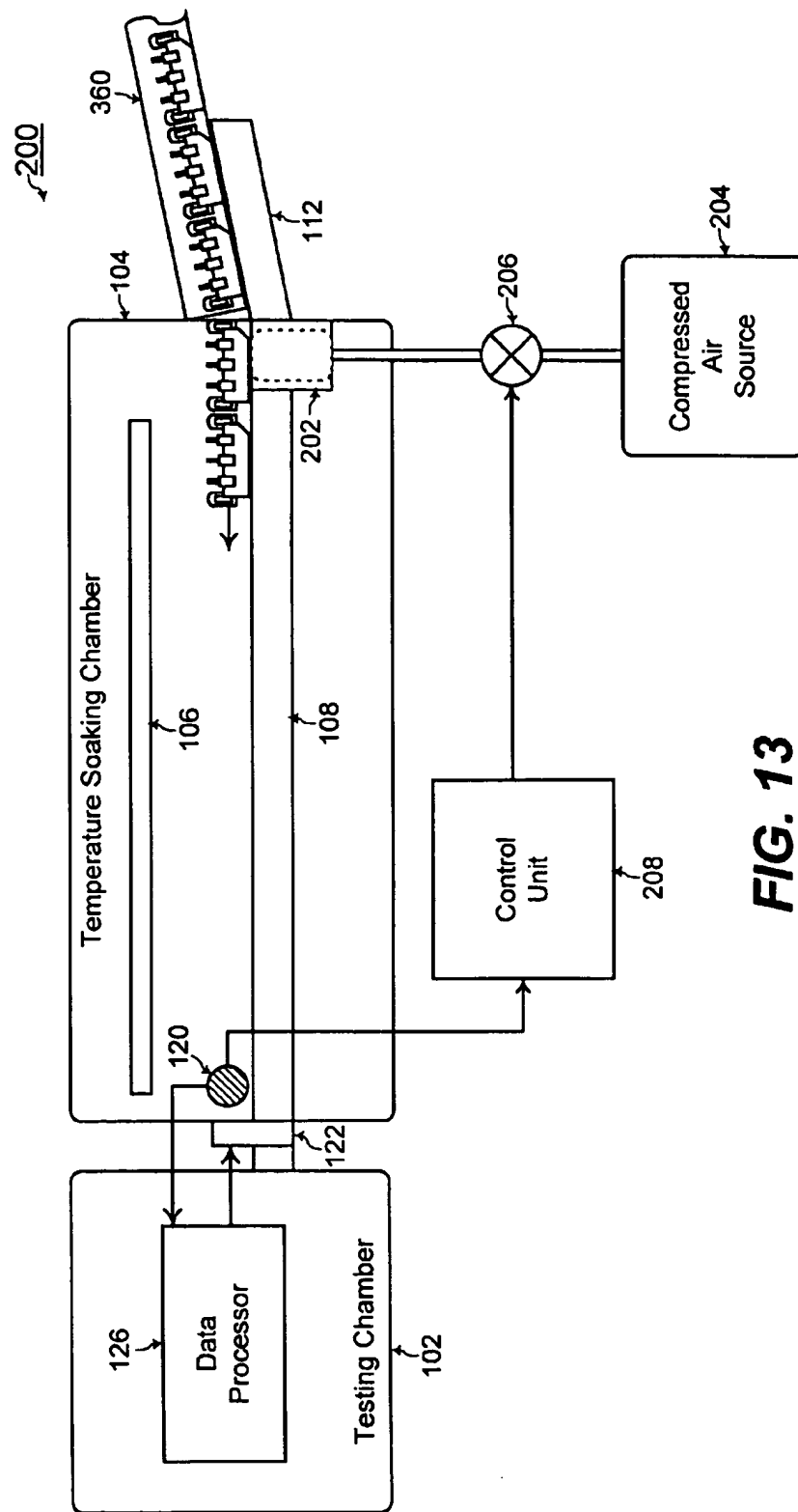


FIG. 13

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AUTOMATED PREVENTION OF TRANSFER OF AN UNSOAKED IC PACKAGE FROM A TEMPERATURE SOAKING CHAMBER TO A TESTING CHAMBER

TECHNICAL FIELD

The present invention relates generally to manufacture of IC (integrated circuit) packages, and more particularly, to a mechanism for automatically preventing the transfer of an IC package from a temperature soaking chamber to a testing chamber when the IC package has not been placed within the temperature soaking chamber for a predetermined time period.

BACKGROUND OF THE INVENTION

Referring to FIG. 1, during manufacture of IC (integrated circuit) packages, the IC packages are tested for proper functionality at a range of temperatures such as from about -40° Celsius to about +85° Celsius, for example. An example testing system that handles the IC packages for such testing of the IC packages for a range of temperatures is the MCT3608E Handler or the MCT3608CCA Handler available from Micro Component Technology, Inc. headquartered in St. Paul, Minn.

Referring to FIG. 1, such a temperature testing system 100 includes a testing chamber 102 and a temperature soaking chamber 104 having a heating or cooling grid 106. The heating or cooling grid 106 is heated or cooled such that the temperature within the soaking chamber 104 is at a predetermined temperature. IC packages are heated or cooled to the predetermined temperature within the soaking chamber 104 by placing the IC packages within the soaking chamber 104 for a predetermined time period. Such a process of heating or cooling the IC packages within the soaking chamber 104 is referred to as "soaking" the IC packages by one of ordinary skill in the art of IC package manufacture.

After the IC packages have been heated or cooled to the predetermined temperature within the soaking chamber 104, the IC packages are transferred to the testing chamber 102 for testing of electrical characteristics of the IC packages when the IC packages are at that predetermined temperature, as known to one of ordinary skill in the art of IC package manufacture. Referring to FIG. 1, the temperature testing system 100 includes a plurality of tracks including a first track 108 and a second track 110 for holding the IC packages through the temperature soaking chamber 104 to the testing chamber 102. A temperature testing system, such as the MCT3608E Handler or the MCT3608CCA Handler available from Micro Component Technology, Inc., typically includes more numerous tracks, such as thirteen tracks for example, but two tracks 108 and 110 are shown in FIG. 1 for clarity of illustration.

Each of the tracks 108 and 110 includes a respective input with a first input 112 for the first track 108 and a second input 114 for the second track 110. A container such as an IC tube for holding the IC packages is placed on the input of a track for transferring the IC packages from the container to the temperature soaking chamber 104. Referring to FIG. 1, a first prior IC tube 116 is placed on the first input 112 of the first track 108, and a second prior IC tube 118 is placed on the second input 114 of the second track 110. Referring to FIGS. 1 and 2, the IC packages from the first prior IC tube 112 are transferred to the first track 108 within the soaking chamber 104, and the IC packages from the second prior IC

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tube 114 are transferred to the second track 110 within the soaking chamber 104. Elements having the same reference number in FIGS. 1 and 2 refer to elements having similar structure and function.

Referring to FIG. 3, a side view of the temperature testing system 100 shows the IC packages, from the first prior IC tube 116 placed at the first input 112, sliding out of the first prior IC tube 116 and onto the first track 108 within the temperature soaking chamber 104. The side view of any track of the temperature testing system 100 including the second track 110 is similar to the side view of the first track 108 as illustrated in FIG. 3. Elements having the same reference number in FIGS. 1, 2, and 3 refer to elements having similar structure and function. An IC package detector 120 is disposed within the temperature soaking chamber near a first output stopper device 122 at the output of the first track 108. Referring to FIGS. 1 and 2, the first output stopper device 122 is at the output of the first track 108, and the second output stopper device 124 is at the output of the second track 110. The output of a track is the end of the track within the soaking chamber 104 near the testing chamber 102.

Referring to FIGS. 3 and 4, the IC package detector 120 is a position sensor such as an opto-electronic position sensor that detects when an object is adjacent to the IC package detector 120. Such position sensors are known to one of ordinary skill in the art of electronics. Referring to FIG. 4, when the track 108 is full of IC packages with an IC package being adjacent the IC package detector 120, the IC package detector 120 sends an "IC package PRESENT" control signal to a data processor 126 of the temperature testing system 100 to indicate that the soaking chamber 104 is full of newly transferred IC packages. Elements having the same reference number in FIGS. 1, 2, 3, and 4 refer to elements having similar structure and function.

The data processor 126 then starts a timer that times up to a predetermined time period from when the IC package detector 120 sends the "IC package PRESENT" control signal to the data processor 126 such that the IC packages on the track 108 are "soaked" to the predetermined temperature of the soaking chamber 104 by being placed within the soaking chamber 104 for the predetermined time period. For example, the predetermined time period may be about 4 minutes.

Referring to FIG. 5, after the predetermined time period from when the IC package detector 120 sends the "IC package PRESENT" control signal, the data processor 126 controls the output stopper device to be lowered to a passing position such that the IC packages on the track 108 may be transferred to the testing chamber 102. The IC packages are then transferred from the soaking chamber 104 to the testing chamber 102 for electrical testing of the IC packages at the predetermined temperature. Elements having the same reference number in FIGS. 1, 2, 3, 4, and 5 refer to elements having similar structure and function.

Referring to FIGS. 3, 5, and 6, as the IC packages of the first prior IC tube 116 are transferred to the testing chamber 102 after such IC packages have been soaked within the soaking chamber 104 for the predetermined time period, a subsequent IC tube 130 may be placed on the input 112 of the track 108. Elements having the same reference number in FIGS. 1, 2, 3, 4, 5, and 6 refer to elements having similar structure and function. The elements of the prior art temperature testing system 100, such as the elements of the MCT3608E Handler or the MCT3608CCA Handler available from Micro Component Technology, Inc., of FIGS. 1,

2, 3, 4, 5, and 6 are known to one of ordinary skill in the art of IC package manufacture

In the prior art temperature testing system 100, an operator keeps track of when the IC packages of the subsequent IC tube 130 are to be placed within the soaking chamber 104 after each of the IC packages of the first prior IC tube 116 has been transferred to the testing chamber 102. However, the operator may erroneously place the subsequent IC tube 130 of IC packages on the input 112 of the track 108 before each of the IC packages of the first prior IC tube 116 has been transferred to the testing chamber 102 as illustrated in FIG. 6.

In that case, the IC packages of the subsequent IC tube 130 are transferred onto the track 108 and may be transferred to the testing chamber 102 without being soaked within the soaking chamber 104 for the predetermined time period. The IC packages of the subsequent IC tube 130 that have not been properly soaked to the predetermined temperature of the soaking chamber 104 are tested in the testing chamber 102 when such IC packages are at an inappropriate temperature resulting in inaccurate testing of such IC packages.

Thus, a mechanism is desired for ensuring that the IC packages of the subsequent IC tube 130 are not transferred to the testing chamber 102 when such IC packages have not been soaked for the predetermined time period within the temperature soaking chamber 104.

SUMMARY OF THE INVENTION

Accordingly, in one embodiment of the present invention, a method and system includes a respective input stopper device at each input of the tracks for ensuring that each of a plurality of IC (integrated circuit) packages are placed within a temperature soaking chamber for the predetermined time period before being transferred to the testing chamber.

In a general aspect of the present invention, an input stopper device is disposed at an input of a track with the track being disposed through the temperature soaking chamber. A prior container holding a prior plurality of IC packages is placed at the input of the track such that the prior plurality of IC packages slides out of the prior container along the track into the soaking chamber when the input stopper device is at a passing position. The prior plurality of IC packages is placed within the soaking chamber for the predetermined time period before each of the prior plurality of IC packages is transferred to the testing chamber when an output stopper device at an output of the track within the soaking chamber is placed to a passing position. A control unit, coupled to the input stopper device, controls the input stopper device to be at a stopping position when any of the prior plurality of IC packages is within the soaking chamber and has not been transferred to the testing chamber. Thus, each of a subsequent plurality of IC packages of a subsequent container is blocked, by the input stopper device, to be contained within the subsequent container placed at the input of the track until each of the prior plurality of IC packages within the soaking chamber has been transferred to the testing chamber.

In addition, the control unit controls the input stopper device to be at the passing position after each of the prior plurality of IC packages has been transferred to the testing chamber and after the output stopper device is placed to a stopping position. Thus, each of the subsequent plurality of IC packages slides from the subsequent container along the track into the soaking chamber. Furthermore, each of the subsequent plurality of IC packages is blocked by the output stopper device from being transferred to the testing chamber

until the subsequent plurality of IC packages has been within the soaking chamber for the predetermined time period.

In another aspect of the present invention, an IC package detector is disposed at the output of the track within the soaking chamber for detecting whether an IC package is present at the output of the track within the soaking chamber. In that case, the control unit controls the input stopper device to be at the stopping position when the IC package detector detects that an IC package is present at the output of the track indicating that any of the prior plurality of IC packages is within the soaking chamber. The output stopper device is placed to a stopping position after the IC package detector detects that no IC package is present at the output of the track. Furthermore, the control unit controls the input stopper device to be at the passing position when the IC package detector detects that no IC package is present at the output of the track and after the output stopper device has been placed to the stopping position.

The present invention may be used to particular advantage when the control unit includes a 5 second timer such that the input stopper device is placed to the stopping position about 5 seconds after the IC package detector begins to detect that an IC package is at the output of the track within the soaking chamber. Thus, all of the prior plurality of IC packages is placed within the soaking chamber before the input stopper device is placed to the stopping position.

Additionally, the control unit may include a 10 second timer such that the input stopper device is placed to the passing position about 10 seconds after the IC package detector begins to detect that no IC package is at the output of the track within the soaking chamber. Thus, the output stopper device is put to the stopping position before the input stopper device is placed to the passing position.

In this manner, each of the IC packages of the subsequent IC package container placed at the input of the track is blocked by the input stopper device from entering the temperature soaking chamber until each of the IC packages of the prior IC package container has been transferred to the testing chamber and until the output stopper device has been placed to the stopping position. After each of the IC packages of the prior IC package container has been transferred to the testing chamber and after the output stopper device has been placed to the stopping position, the input stopper device is placed to the passing position such that the IC packages of the subsequent IC package container are transferred to the soaking chamber. Then, after such IC packages have been within the soaking chamber for the predetermined time period, the output stopper device is placed to the passing position such that the IC packages of the subsequent IC package container are transferred to the testing chamber. Thus, each of the IC packages of the prior IC package container and the subsequent IC package container is placed within the soaking chamber for the predetermined time period before being transferred to the testing chamber for testing of the IC packages at the proper temperature.

These and other features and advantages of the present invention will be better understood by considering the following detailed description of the invention which is presented with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a top view of a temperature testing system of the prior art having a temperature soaking chamber and a testing chamber for testing IC packages at a range of temperatures;

FIG. 2 shows the temperature testing system of FIG. 1 with each of the IC packages transferred from IC tubes to the temperature soaking chamber;

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FIG. 3 shows a side view of the temperature testing system of FIG. 1 as the IC packages from a prior IC tube are transferred into the temperature soaking chamber;

FIG. 4 shows the side view of the temperature testing system of FIG. 3 after each of the IC packages of the prior IC tube has been transferred into the temperature soaking chamber;

FIG. 5 shows the side view of the temperature testing system of FIG. 4 after each of the IC packages of the prior IC tube has been placed within the temperature soaking chamber for a predetermined time period when an output stopper device is placed to a passing position such that the IC packages may be transferred to the testing chamber;

FIG. 6 shows the side view of the temperature testing system of FIG. 5 with transfer of IC packages to the temperature soaking chamber from a subsequent IC tube as the IC packages of the prior IC tube are being transferred to the testing chamber, according to the prior art;

FIG. 7 shows an input stopper device placed at the input of a track into the temperature soaking chamber and a control unit for controlling the input stopper device to block IC packages of the subsequent IC tube from entering the temperature soaking chamber until each of the IC packages of the prior IC tube has been transferred to the testing chamber, according to an embodiment of the present invention;

FIG. 8 shows components of an example circuit of the control unit of FIG. 7 for generating the control signals for controlling the input stopper device of FIG. 7;

FIG. 9 shows a timing diagram of the control signals generated by the control circuit of FIG. 8;

FIG. 10 shows a side view of the temperature testing system with the components of an aspect of the present invention as the input stopper device is placed to a passing position such that the IC packages of the prior IC tube are transferred to the temperature soaking chamber;

FIG. 11 show the side view of the temperature testing system of FIG. 10 after each of the IC packages of the prior IC tube has been transferred to the temperature soaking chamber;

FIG. 12 shows the side view of the temperature testing system of FIG. 11 with the input stopper device being placed at a stopping position as each of the IC packages of the prior IC tube is being transferred to the testing chamber after the IC packages have been within the temperature soaking chamber for the predetermined time period; and

FIG. 13 shows the side view of the temperature testing system of FIG. 12 with the input stopper device being placed to a passing position after each of the IC packages of the prior IC tube has been transferred to the testing chamber.

The figures referred to herein are drawn for clarity of illustration and are not necessarily drawn to scale. Elements having the same reference number in FIGS. 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, and 13 refer to elements having similar structure and function.

DETAILED DESCRIPTION

Referring to FIG. 7, components of a temperature testing system 200 for ensuring that each IC package is soaked within the temperature soaking chamber 104 for the predetermined time period is described and illustrated for the first track 108 as an example track through the temperature soaking chamber 104. However, such respective components may be included for each of the tracks through the temperature soaking chamber 104 for ensuring that each IC

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package through each of the tracks is soaked within the temperature soaking chamber 104 for the predetermined time period before being transferred to the testing chamber 102, as would be apparent to one of ordinary skill in the art of IC package manufacture from the description herein for the example first track 108.

Referring to FIG. 7, the temperature testing system 200 includes the testing chamber 102 and the temperature soaking chamber 104 as described for the temperature testing system 100 of FIGS. 1, 2, 3, 4, 5, and 6 with the same reference number in FIGS. 1, 2, 3, 4, 5, 6, and 7 referring to elements having similar structure and function. However, the temperature testing system 200 includes additional components from the prior art temperature testing system 100 for ensuring that each IC package through each of the tracks is soaked within the temperature soaking chamber 104 for the predetermined time period before being transferred to the testing chamber 102.

In FIG. 7, an input stopper device 202 is included at the input 112 of the track 108 that is placed to a stopping position or a passing position. The input stopper device 202 in one embodiment of the present invention includes a pneumatic cylinder 203 that is raised to be in the stopping position or that is lowered to be in the passing position. In that case, the pneumatic cylinder 203 of the input stopper device 202 is coupled to a compressed air source 204 via an air valve 206. The air valve 206 is adjusted to control the amount of compressed air to the pneumatic cylinder 203 of the input stopper device 202 from the compressed air source 204. The amount of air to the pneumatic cylinder 203 of the input stopper device 202 determines whether the pneumatic cylinder 203 is raised to be in the stopping position or lowered to be in the passing position. Technology for such operation of the pneumatic cylinder 203, the air valve 206, and the compressed air source 204 is known to one of ordinary skill in the art of mechanics.

A control unit 208 is coupled to the air valve 206 for sending a control signal that adjusts the air valve 206 for controlling the amount of compressed air to the pneumatic cylinder 203 from the compressed air source 204. Thus, the control unit 208 controls whether the pneumatic cylinder 203 of the input stopper device 202 is raised to be in the stopping position or lowered to be in the passing position. In addition, the control unit 208 is coupled to the IC package detector 120 for receiving a control signal that is in one of two states, "IC package PRESENT" or "IC package NOT PRESENT," for indicating whether the pneumatic cylinder 203 of the input stopper device 202 is to be raised to be in the stopping position or lowered to be in the passing position.

Referring to FIG. 8, an example embodiment of the control unit 208 includes an "I/P" (input) node 302 that is coupled to the IC package detector 120 for receiving the control signal that is in one of two states, "IC package PRESENT" or "IC package NOT PRESENT." The I/P node 302 is coupled to a five second timer 304 for generating a control signal A at the output node 306 of the five second timer 304. In addition, the I/P node 302 is coupled to a ten second timer 308 via a first inverter 310 to generate a control signal B at the output node 312 of the ten second timer 308.

The I/P node 302 and the output node 312 of the ten second timer 308 are coupled to the inputs of an exclusive OR-gate 314. The output of the exclusive OR-gate 314 is coupled to a second inverter 316 to generate a control signal C at the output node 318 of the second inverter 316. The output node 306 of the five second timer 304 is coupled to

an input of an AND-gate 320 through a third inverter 322, and the output node 318 of the second inverter 316 is the other input to the AND-gate 320, to generate a control signal D at the output node 323 of the AND-gate 320. The output node 312 of the ten second timer 308 and the output node 323 of the AND-gate 320 are coupled as inputs of an OR-gate 324 to generate an output Control signal at the output node 326 of the OR-gate 324. The output node 326 of the OR-gate 324 is coupled to the air valve 206. Logic gates such as exclusive OR-gates, AND-gates, OR-gates, and inverters are known to one of ordinary skill in the art of electronics.

During operation of the temperature testing system 200 of an embodiment of the present invention, FIG. 9 shows a timing diagram of the controls signals generated by the control unit 208 of FIG. 8. Referring to FIG. 9, a first signal 332 ("I/P") of the timing diagram of FIG. 9 is the control signal I/P at the input node 302, and a second signal 334 is the inverse of the first signal 332. A third signal ("Signal A") 336 is the control signal A at the output node 306 of the five second timer 304, and a fourth signal 338 is the inverse of the third signal 336. A fifth signal 340 ("Signal B") is the control signal B at the output node 312 of the ten second timer 308. A sixth signal 342 ("Signal C") is the control signal C at the output node 318 of the second inverter 316. A seventh signal 344 ("Signal D") is the control signal D at the output node 323 of the AND-gate 320, and an eighth signal 346 ("Output") is the output control signal at the output node 326 of the OR-gate 324.

Referring to FIGS. 7, 8, 9, and 10, before a first time point 352, the control signal I/P at the I/P node 302 from the IC package detector 120 is at the "IC package NOT PRESENT" (i.e., high) state indicating that no IC package is present on the track 108 within the temperature soaking chamber 104. Thus, before the time point 352, the output control signal at the output node 326 of the OR-gate 324 is low. The output node 326 of the OR-gate 324 is coupled to the air valve 206, and when the output control signal at the output node 326 is low, the air valve 206 is closed to minimize the amount of compressed air to the pneumatic cylinder 203 of the input stopper device 202 from the compressed air source 204.

With minimized amount of compressed air to the pneumatic cylinder 203, the pneumatic cylinder 203 is lowered to be at the passing position. Referring to FIG. 10, when the pneumatic cylinder 203 is lowered to be at the passing position, a prior plurality of IC packages within a prior IC tube 354 placed at the input 112 of the track 108 slides out from the prior IC tube 354 and onto the track 108 within the temperature soaking chamber 104. Referring to FIGS. 10 and 11, when each of the prior plurality of IC packages of the prior IC tube 354 are transferred to the track 108 within the soaking chamber 104, an IC package is adjacent the IC package detector 120.

In that case, the control signal at the I/P node 302 from the IC package detector turns to the "IC package PRESENT" (i.e., low) state at time point 352 in the timing diagram of FIG. 9. Referring to FIG. 9, after the control signal 332 at the I/P node 302 from the IC package detector turns to the "IC package PRESENT" (i.e., low) state at time point 352, the transition of the control signal 332 at the I/P node 302 from a high state to a low state causes the five second timer 304 to generate a pulse 356 that is high for a time period of five seconds for the control signal A (336 in FIG. 9). The control signal A turns high at the transition of the control signal 332 at the I/P node 302 from a high state to a low state. The control signal A is generated by the five second timer 304 and turns back low after five seconds from when the control

signal A turned high. Timer circuits of the five second timer 304 for generating such a control signal A are known to one of ordinary skill in the art of electronics.

Further referring to FIG. 9, with generation of such a control signal A, the output control signal 346 at the output node 326 of the OR-gate 324 turns high at time point 358 which is five seconds after the transition of the control signal 332 at the I/P node 302 from a high state to a low state (i.e. time point 352). Referring to FIGS. 9 and 11, the output node 326 of the OR-gate 324 is coupled to the air valve 206, and when the output control signal at the output node 326 is high, the air valve 206 is opened to maximize the amount of compressed air to the pneumatic cylinder 203 of the input stopper device 202 from the compressed air source 204. With maximized amount of compressed air to the pneumatic cylinder 203, the pneumatic cylinder 203 is raised to be at the stopping position. The five second delay in the output control signal 346 turning high at time point 358 after the transition of the control signal 332 ensures that all of the prior plurality of IC packages of the prior IC tube 354 is transferred out of the prior IC tube 354 to the track 108 before the pneumatic cylinder 203 is raised to the stopping position.

Referring to FIG. 11, the IC package detector 120 also sends the "IC package PRESENT" control signal to the data processor 126 of the temperature testing system 200 as also described for the prior art temperature testing system 100. The data processor 126 then begins to time up to a predetermined time period from receiving the "IC package PRESENT" control signal to control the output stopper device 122 to be raised to a stopping position during the predetermined time period such that each of the plurality of IC packages of the prior IC tube 354 soaks up to the predetermined temperature within the soaking chamber 104 before being passed to the testing chamber 102.

Referring to FIG. 12, after the data processor 126 times up to the predetermined time period from receiving the "IC package PRESENT" control signal, the data processor 126 controls the output stopper device 122 to be lowered to a passing position such that each of the prior plurality of IC packages of the prior IC tube 354 is passed to the testing chamber 102. Each IC package passes adjacent the IC package detector 120 as the IC package is transferred from the soaking chamber 104 to the testing chamber 102. Thus, the I/P control signal from the IC package detector 120 remains in the "IC package PRESENT" (i.e., low in FIG. 9) state until each of the prior plurality of IC packages of the prior IC tube 354 is passed to the testing chamber 102. The IC package detector 120 determines whether any of the prior plurality of IC packages of the prior IC tube 354 is still within the soaking chamber 104.

Referring to FIG. 13, when each of the prior plurality of IC packages of the prior IC tube 354 has been passed to the testing chamber 102 from the soaking chamber 104, no IC package of the prior plurality of IC packages of the prior IC tube 354 is adjacent the IC package detector 120 within the soaking chamber 104. In that case, referring to FIG. 9, the I/P control signal from the IC package detector 120 transitions to the "IC package NOT PRESENT" (i.e., high in FIG. 9) state at time point 362. The time duration from time point 352 to the time point 362 depends on the predetermined time duration for soaking the IC packages within the soaking chamber 104 as timed by the data processor 126 (such as 4 minutes for the MCT3608E Handler available from Micro Component Technology, Inc. for example) and the time duration for transferring each of the prior plurality of IC packages of the prior IC tube 354 from the soaking chamber

104 to the testing chamber 102 (such as 6 minutes for the MCT3608E Handler available from Micro Component Technology, Inc. for example).

At time point 362 when the I/P control signal from the IC package detector 120 transitions from the low state to the high state, the ten second timer 308 generates a pulse 364 that is high for a time period of ten seconds for the control signal B (340 in FIG. 9). The control signal B turns high at the transition of the control signal 332 at the I/P node 302 from a low state to a high state. The control signal B is generated by the ten second timer 308 and turns back low after ten seconds from when the control signal B turned high. Timer circuits of the ten second timer 308 for generating such a control signal B are known to one of ordinary skill in the art of electronics.

Further referring to FIG. 9, with generation of such a control signal B, the output control signal 346 at the output node 326 of the OR-gate 324 turns low at time point 366 which is ten seconds after the transition of the control signal 332 at the I/P node 302 from a low state to a high state (i.e. time point 362). Referring to FIGS. 9 and 13, the output node 326 of the OR-gate 324 is coupled to the air valve 206, and when the output control signal at the output node 326 is low, the air valve 206 is closed to minimize the amount of compressed air to the pneumatic cylinder 203 of the input stopper device 202 from the compressed air source 204. With minimized amount of compressed air to the pneumatic cylinder 203, the pneumatic cylinder 203 is lowered to be at the passing position.

The ten second delay in the output control signal 346 turning low at time point 366 after the transition of the control signal 332 ensures that the output stopper device 122 is raised to the stopping position by the data processor 126 before the pneumatic cylinder 203 is lowered to the passing position. Referring to FIGS. 9 and 13, when each of the prior plurality of IC packages of the prior IC tube 354 has been passed to the testing chamber 102 from the soaking chamber 104, the IC package detector 120 also sends the "IC package NOT PRESENT" control signal at time point 362 to the data processor 126. The data processor 126 controls the output stopper device 122 to be raised to the stopping position within ten seconds from receiving the "IC package NOT PRESENT" control signal at time point 362 such that the output stopper device 122 is raised to the stopping position before the pneumatic cylinder 203 is raised to the passing position.

In this manner, referring to FIGS. 11, 12, and 13, each of the IC packages within a subsequent IC tube 360 placed at the input 112 of the track 108 is blocked by the pneumatic cylinder 203 of the input stopper device 202 from entering the temperature soaking chamber 104 until each of the IC packages of the prior IC tube 354 has been transferred to the testing chamber 102 and until the output stopper device 122 has been placed to the stopping position. Thus, any of the IC packages of the subsequent IC tube 360 is prevented from being transferred to the testing chamber 102 without being soaked within the soaking chamber 104 for the predetermined time period as the IC packages of the prior IC tube 354 are being transferred to the testing chamber 102.

After each of the IC packages of the prior IC tube 354 has been transferred to the testing chamber 102 from the soaking chamber 104 and after the output stopper device 122 has been placed to the stopping position, the input stopper device 202 is placed to the passing position such that the IC packages of the subsequent IC tube 360 may be transferred to the soaking chamber 104. The output stopper device 122

that is in the stopping position blocks the IC packages of the subsequent IC tube 360 from passing to the testing chamber 102. Then, after such IC packages have been within the soaking chamber 104 for the predetermined time period, the output stopper device 122 is placed to the passing position such that the IC packages of the subsequent IC tube 360 are transferred to the testing chamber 102. Thus, each of the IC packages of the prior IC tube 354 and the subsequent IC tube 360 is placed within the soaking chamber 104 for the predetermined time period before being transferred to the testing chamber 102 for testing of the IC packages at the proper temperature.

Referring to FIG. 9, the I/P control signal from the IC package detector 120 remains high from time point 362 until time point 368 while any of the IC packages of the subsequent IC tube 360 are adjacent the IC package detector 120 within the soaking chamber 104 for the predetermined time period and then as such IC packages are transferred to the testing chamber 102. When each of the IC packages of the subsequent IC tube 360 has been transferred to the testing chamber 102 with no IC package being adjacent the IC package detector 120, the I/P control signal from the IC package detector 120 transitions from a high state to a low state at time point 368, and the process repeats again as described from time point 352 for IC packages from another IC tube placed at the input 112.

The foregoing is by way of example only and is not intended to be limiting. For example, components of a temperature testing system 200 for ensuring that each IC package is soaked within the temperature soaking chamber 104 for the predetermined time period is described and illustrated for the first track 108 as an example track through the temperature soaking chamber 104. However, such respective components may be included for each of the tracks through the temperature soaking chamber 104 for ensuring that each IC package through each of the tracks is soaked within the temperature soaking chamber 104 for the predetermined time period before being transferred to the testing chamber 102, as would be apparent to one of ordinary skill in the art of IC package manufacture from the description herein for the example first track 108.

The present invention is limited only as defined in the following claims and equivalents thereof.

We claim:

1. A system for ensuring that each of a plurality of IC (integrated circuit) packages are placed within a temperature soaking chamber for a predetermined time period before being transferred to a testing chamber, the system comprising:

an input stopper device disposed at an input of a track, wherein said track is disposed through said soaking chamber, and wherein a prior container holding a prior plurality of IC packages is placed at said input of said track such that said prior plurality of IC packages slides out of said prior container along said track into said soaking chamber when said input stopper device is at a passing position;

and wherein said prior plurality of IC packages is placed within the soaking chamber for said predetermined time period before each of said prior plurality of IC packages is transferred to said testing chamber when an output stopper device at an output of said track within said soaking chamber is placed to a passing position; and

a control unit, coupled to said input stopper device, for controlling said input stopper device to be at a stopping

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position when any of said prior plurality of IC packages is within said soaking chamber and has not been transferred to said testing chamber such that each of a subsequent plurality of IC packages within a subsequent container is blocked, by said input stopper device, to be contained within said subsequent container placed at said input of said track until each of said prior plurality of IC packages within said soaking chamber has been transferred to said testing chamber; and wherein said control unit controls said input stopper device to be at said passing position after each of said prior plurality of IC packages has been transferred to said testing chamber and after said output stopper device is placed to a stopping position such that each of said subsequent plurality of IC packages slides from said soaking chamber and such that each of said subsequent plurality of IC packages is blocked by said output stopper device from being transferred to said testing chamber until said subsequent plurality of IC packages has been within said soaking chamber for said predetermined time period.

2. The system of claim 1, further comprising:

an IC package detector disposed at said output of said track within said soaking chamber for detecting whether an IC package is present at said output of said track within said soaking chamber;

wherein said control unit controls said input stopper device to be at said stopping position when said IC package detector detects that an IC package is present at said output of said track indicating that any of said prior plurality of IC packages is within said soaking chamber;

and wherein said output stopper device is placed to a stopping position after said IC package detector detects that no IC package is present at said output of said track;

and wherein said control unit controls said input stopper device to be at said passing position when said IC package detector detects that no IC package is present at said output of said track and after said output stopper device has been placed to said stopping position.

3. The system of claim 2, wherein said control unit includes a 5 second timer such that said input stopper device is placed to said stopping position about 5 seconds after said IC package detector begins to detect that an IC package is at said output of said track within said soaking chamber such that all of said prior plurality of IC packages is placed within said soaking chamber before said input stopper device is placed to said stopping position.

4. The system of claim 2, wherein said control unit includes a 10 second timer such that said input stopper device is placed to said passing position about 10 seconds after said IC package detector begins to detect that no IC package is at said output of said track within said soaking chamber such that said output stopper device is put to said stopping position before said input stopper device is placed to said passing position.

5. The system of claim 1, wherein said input stopper device is a pneumatic cylinder, disposed at said input of said track, that is raised to be at said stopping position and that is lowered to be at said passing position.

6. A system for ensuring that each of a plurality of IC (integrated circuit) packages are placed within a temperature soaking chamber for a predetermined time period before being transferred to a testing chamber, the system comprising:

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an input stopper device disposed at an input of a track, wherein said track is disposed through said soaking chamber, and wherein a prior container holding a prior plurality of IC packages is placed at said input of said track such that said prior plurality of IC packages slides out of said prior container along said track into said soaking chamber when said input stopper device is at a passing position;

and wherein said prior plurality of IC packages is placed within the soaking chamber for said predetermined time period before each of said prior plurality of IC packages is transferred to said testing chamber when an output stopper device at an output of said track within said soaking chamber is placed to a passing position;

means for controlling said input stopper device to be at a stopping position when any of said prior plurality of IC packages is within said soaking chamber and has not been transferred to said testing chamber such that each of a subsequent plurality of IC packages within a subsequent container is blocked, by said input stopper device, to be contained within said subsequent container placed at said input of said track until each of said prior plurality of IC packages within said soaking chamber has been transferred to said testing chamber until said subsequent plurality of IC packages has been within said soaking chamber for said predetermined time period; and

means for controlling said input stopper device to be at said passing position after each of said prior plurality of IC packages has been transferred to said testing chamber and after said output stopper device is placed to a stopping position such that each of said subsequent plurality of IC packages slides from said subsequent container along said track into said soaking chamber and such that each of said subsequent plurality of IC packages is blocked by said output stopper device from being transferred to said testing chamber.

7. The system of claim 6, further comprising:

an IC package detector disposed at said output of said track within said soaking chamber for detecting whether an IC package is present at said output of said track within said soaking chamber;

means for controlling said input stopper device to be at said stopping position when said IC package detector detects that an IC package is present at said output of said track indicating that any of said prior plurality of IC packages is within said soaking chamber;

and wherein said output stopper device is placed to a stopping position after said IC package detector detects that no IC package is present at said output of said track; and

means for controlling said input stopper device to be at said passing position when said IC package detector detects that no IC package is present at said output of said track and after said output stopper device has been placed to said stopping position.

8. The system of claim 7, further comprising:

means for controlling said input stopper device to be placed to said stopping position about 5 seconds after said IC package detector begins to detect that an IC package is at said output of said track within said soaking chamber such that all of said prior plurality of IC packages is placed within said soaking chamber before said input stopper device is placed to said stopping position.

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9. The system of claim 7, further comprising:

means for controlling said input stopper device to be placed to said passing position about 10 seconds after said IC package detector begins to detect that no IC package is at said output of said track within said soaking chamber such that said output stopper device is put to said stopping position before said input stopper device is placed to said passing position.

10. The system of claim 6, wherein said input stopper device is a pneumatic cylinder, disposed at said input of said track, that is raised to be at said stopping position and that is lowered to be at said passing position.

11. A method for ensuring that each of a plurality of IC (integrated circuit) packages are placed within a temperature soaking chamber for a predetermined time period before being transferred to a testing chamber, the system comprising:

controlling an input stopper device disposed at an input of a track to be placed to a passing position, wherein said track is disposed through said soaking chamber, such that a prior plurality of IC packages from a prior container placed at said input of said track slides out of said prior container along said track into said soaking chamber;

wherein said prior plurality of IC packages are soaked within the soaking chamber for said predetermined time period before each of said prior plurality of IC packages is transferred to said testing chamber when an output stopper device at an output of said track within said soaking chamber is placed to a passing position;

controlling said input stopper device to be at a stopping position when any of said prior plurality of IC packages is within said soaking chamber and has not been transferred to said testing chamber such that each of a subsequent plurality of IC packages within a subsequent container is blocked, by said input stopper device, to be contained within said subsequent container placed at said input of said track until each of said prior plurality of IC packages within said soaking chamber has been transferred to said testing chamber; and

controlling said input stopper device to be at said passing position after each of said prior plurality of IC packages has been transferred to said testing chamber and after said output stopper device is placed to a stopping position such that each of said subsequent plurality of IC packages slides from said subsequent container along said track into said soaking chamber and such

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that each of said subsequent plurality of IC packages is blocked by said output stopper device from being transferred to said testing chamber until said subsequent plurality of IC packages has been within said soaking chamber for said predetermined time period.

12. The method of claim 11, further including the steps of: detecting whether an IC package is present at said output of said track within said soaking chamber;

controlling said input stopper device to be at said stopping position when an IC package is detected to be present at said output of said track indicating that any of said prior plurality of IC packages is within said soaking chamber;

wherein said output stopper device is placed to a stopping position after said IC package detector detects that no IC package is present at said output of said track; and

controlling said input stopper device to be at said passing position when no IC package is detected to be present at said output of said track and after said output stopper device has been placed to said stopping position.

13. The method of claim 12, further including the step of:

controlling said input stopper device to be placed to said stopping position about 5 seconds after an IC package is detected at said output of said track within said soaking chamber such that all of said prior plurality of IC packages is placed within said soaking chamber before said input stopper device is placed to said stopping position.

14. The method of claim 12, further including the step of:

controlling said input stopper device to be placed to said passing position about 10 seconds after no IC package is detected at said output of said track within said soaking chamber such that said output stopper device is put to said stopping position before said input stopper device is placed to said passing position.

15. The method of claim 11, wherein said input stopper device is a pneumatic cylinder disposed at said input of said track, and wherein said method further includes the steps of:

raising said pneumatic cylinder to be at said stopping position to block any IC packages from passing to said soaking chamber from a container placed at said input of said track; and

lowering said pneumatic cylinder to be at said passing position to transfer IC packages to said soaking chamber from a container placed at said input of said track.

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